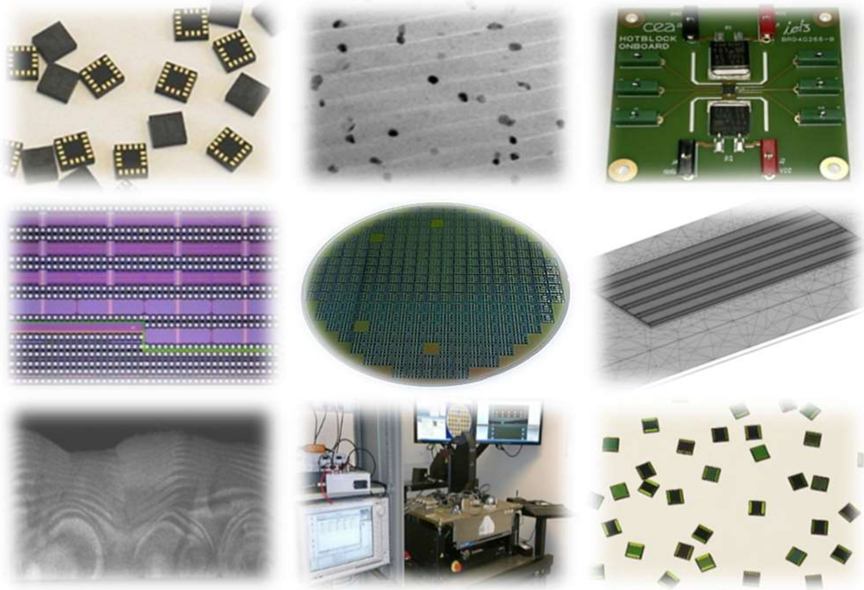

DEVELOPMENT OF INTEGRATED MICRO-THERMOELECTRIC SENSORS FOR IC APPLICATIONS

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Caen – France / 1-5 July 2018

OUTLOOK

1 – Definitions and principles

2 – µThermoElectric Sensors technologies

- In-IC µTES
- Stand-alone µTES
- On-interposer µTES

3 – Conclusions & perspectives

1 – Definitions and principles

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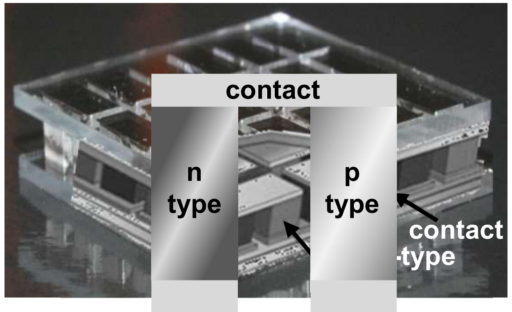
3 – Conclusions & perspectives

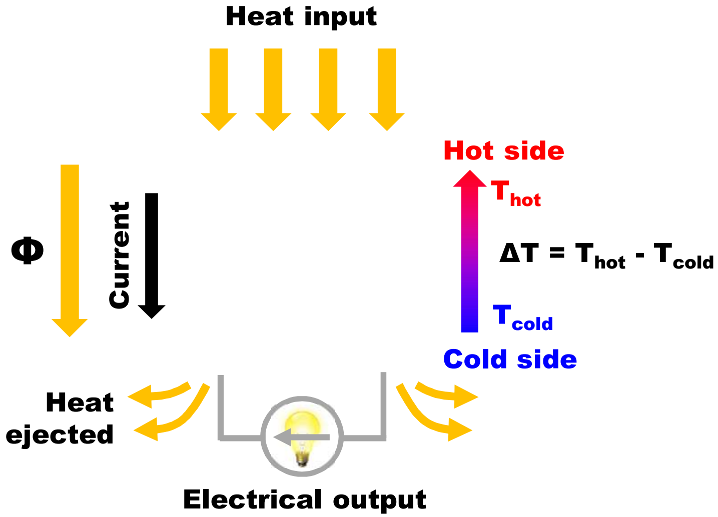
DEFINITIONS

- **What is a thermoelectric sensor?**

  → Thermoelectric device using Seebeck effect to convert a thermal signal to an electrical signal

Standard structure of TE device in bulk technology.





- **To measure what?**

  → Measurement of thermal flow Φ

  → Measurement of temperature difference ΔT

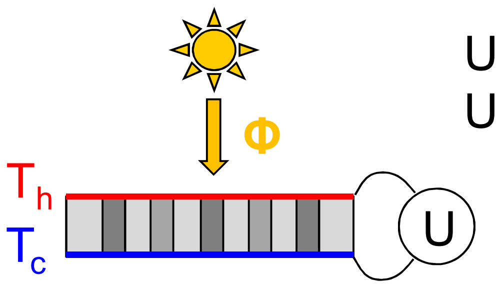
- **For what kind of applications?**

  → Thermal management in microelectronic environment, home automation, automotive, etc.

PRINCIPLE

- **Working mode of thermoelectric sensor**

  → based on Seebeck effect



Schematic cross view of TE sensor

$U = N \times S_{np} \times \Delta T$

$U = N \times S_{np} \times R_{th} \times \Phi$

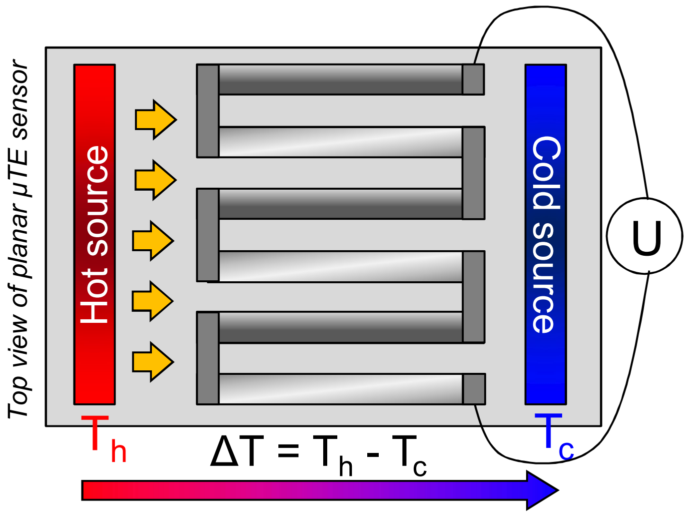
with

U = generated voltage (V)
N = junctions number (-)
S_{np} = Seebeck coefficient of one junction (µV/K)
R_{th} = thermal resistance (K/W)

- **µTES: TE sensors in thin film technology**

  → planar sensors (2D)

  → key parameters:
  - . sensitivity S_e (mV/K)
  - . area A_{TE} (mm²)
  - . electrical resistance R_{el} (Ω)
  - . thermal resistance R_{th} (K/W)
  - . response time t (s)



→ µTES performance depend on materials, geometry and environment

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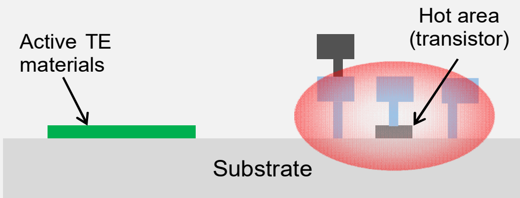
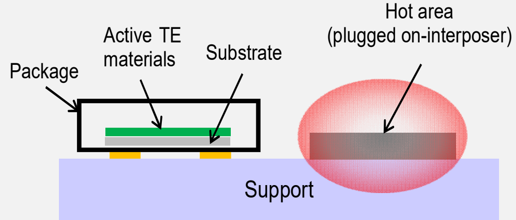
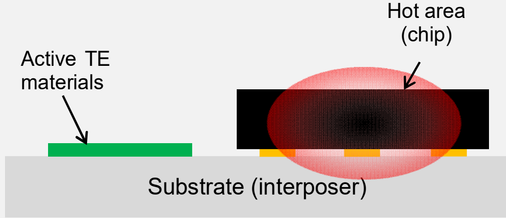
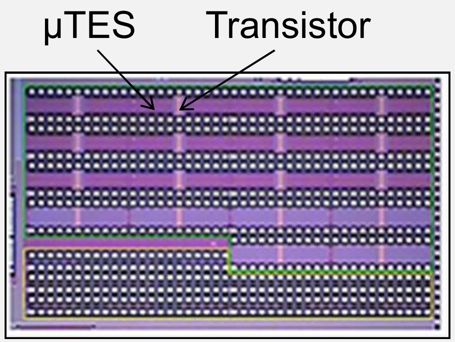
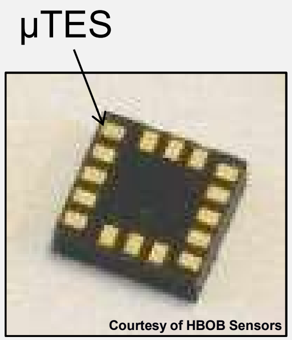
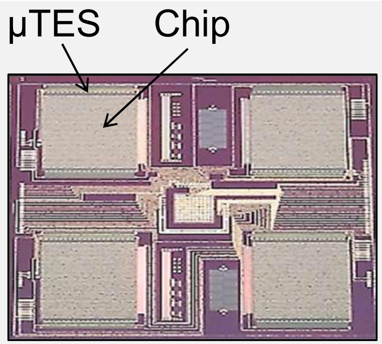
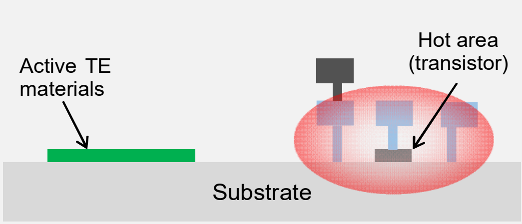
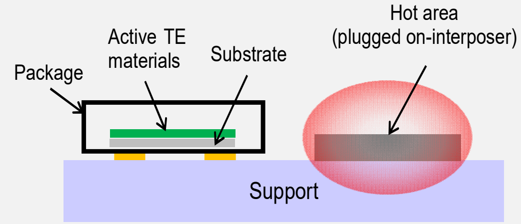
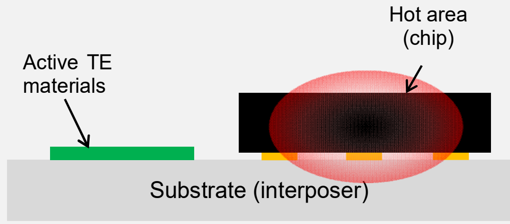
µTES TECHNOLOGIES

- **Three main technologies for thin film TE sensors**

Technology	"in-IC"	"stand-alone"	"on-interposer"
Schematics			
Pictures			
Main characteristics	Integrated sensors manufactured in CMOS technology, as the same time than CMOS transistors	Packaged sensors manufactured in microelectronic technology, independently of the final application, to be used in any conditions	Unpackaged integrated sensors manufactured in microelectronic technology, independently of the final application

µTES TECHNOLOGIES

- **Three main technologies for thin film TE sensors**

<table>
<tr><th>Technology</th><th>“in-IC”</th><th>“stand-alone”</th><th>“on-interposer”</th></tr>
<tr><td>Schematics</td><td>
</td><td>
</td><td>
</td></tr>
<tr><td>Field</td><td>Microelectronic applications</td><td>Any kind of applications (microelectronic, transport, home/building automation…)</td><td>Microelectronic applications</td></tr>
<tr><td>Advantages</td><td>µTES can be integrated at the nearest of hot points to control (typically CMOS transistors)</td><td>µTES can be manufactured with a high flexibility in the process flow, enabling to optimize µTES independently from the environment</td><td>µTES can be integrated at the nearest of hot points with a high flexibility in the process flow</td></tr>
</table>

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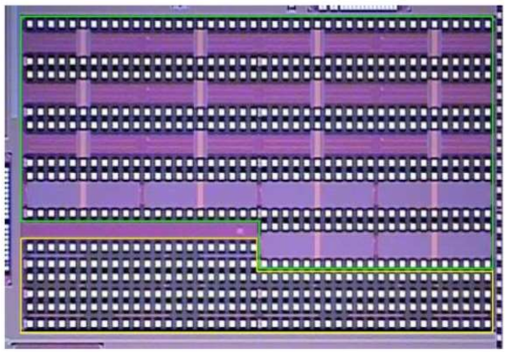
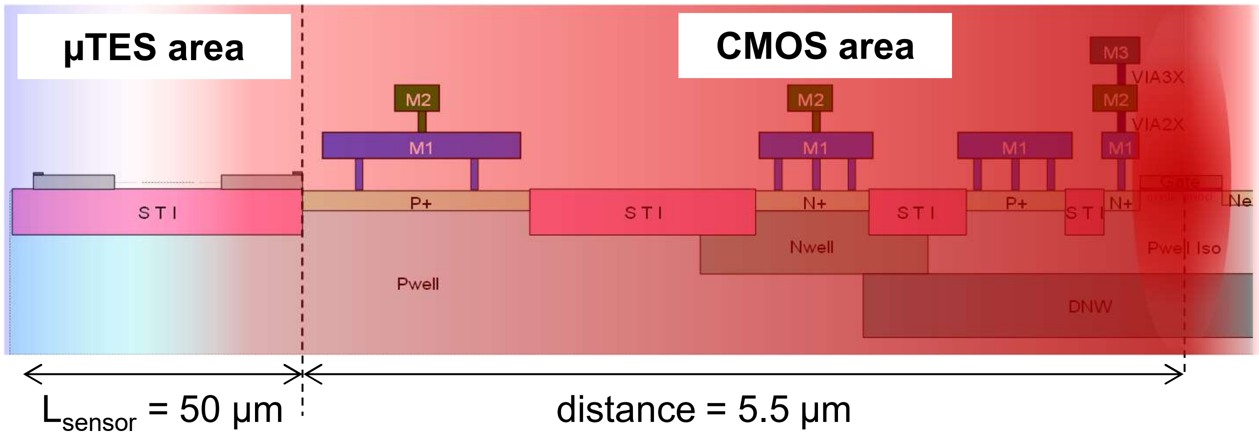
IN-IC µTES

- **Strategy**
  - Thermal management from integrated sensors located at the nearest from critical area (chips, transistors…)
  - Sensors developed in CMOS (C065 et C040) technology without any change in the process flow *
  - µTES sensitivity 50% higher than Intel thermal sensors, without supply current

µTES in C065 technology (top view)



µTES integration in CMOS technology (cross view)

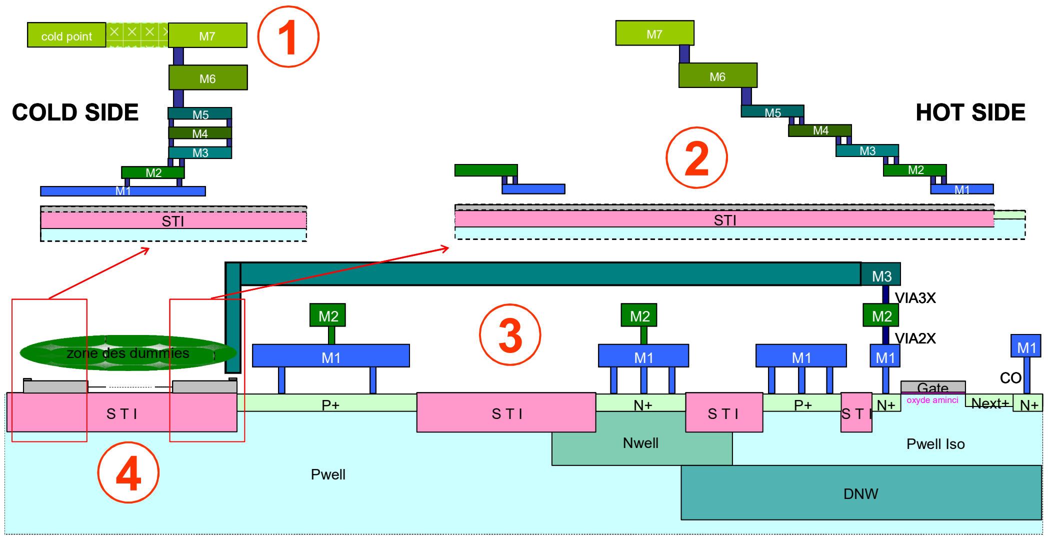


** Patent WO2011012586*
Patent WO2012131183

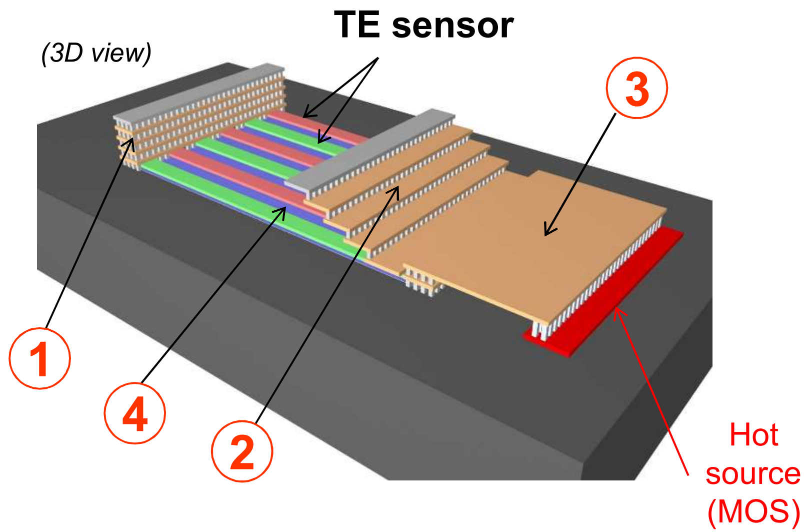
IN-IC µTES

- **Specific in-IC µTES design**

→ Optimization of hot and cold sides to increase the temperature difference *



(cross section)



1 - cold side : "ladder" structure connected to a cold point to drain the heat

2 - hot side : "stairs" structure to deviate the thermal flow diffusion from the hot to cold side by using dummies levels

3 - metallic "bridge" between the sensor hot side and the MOS to an increase of sensitivity and response time

4 - STI : all along the structure to delay the heat diffusion from hot side to cold side

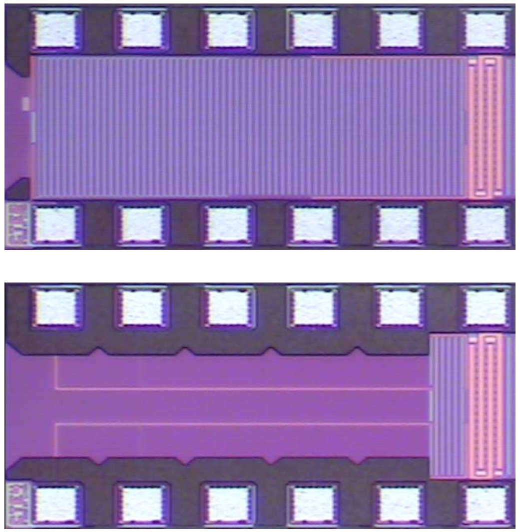
* Patent WO2011012586

- **In-IC µTES characteristics**

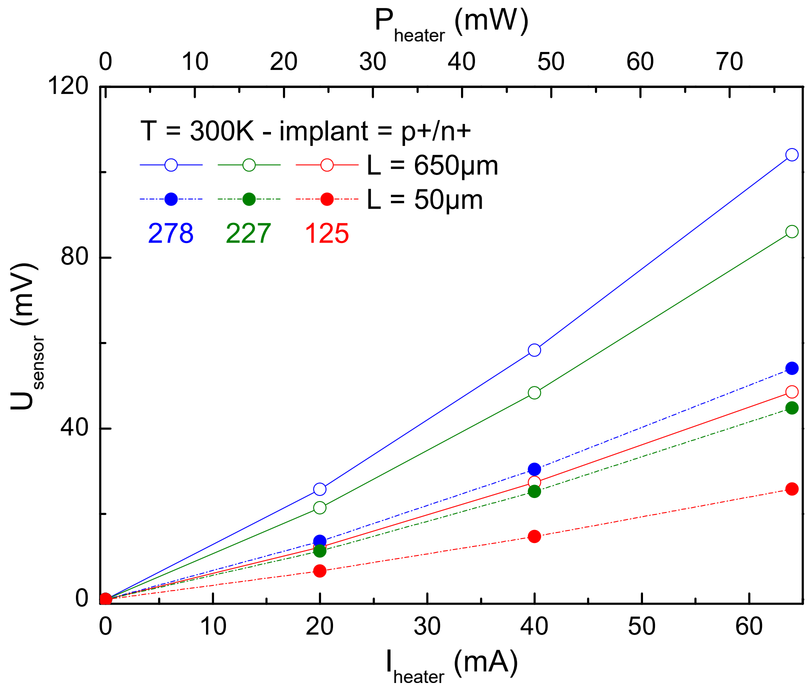
→ TE materials: doped poly-Si (corresponding to the CMOS gate material)

→ Tests in different configurations (temperature, steady or dynamic state)

→ Tests of several geometries (sensors length, junctions number, etc.)



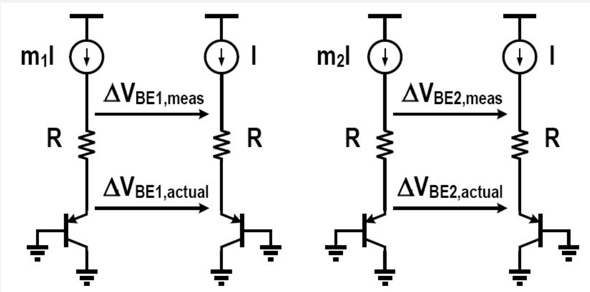
Top view of in-IC µTES with 650 µm and 50 µm length



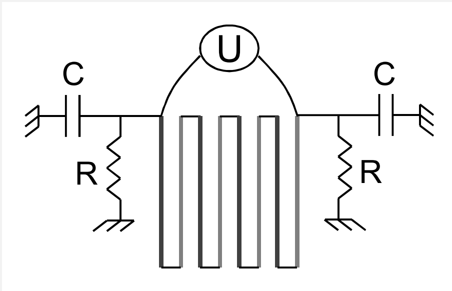
Example of µTES signal depending on power of heater (transistor) for different sensors

- **Comparison with SoA in-IC thermal sensors**

BJT sensors (Intel)	µTES (CEA)
- sensitivity: 140 µV/K - need analogic polarization current - need 2 sensors to measure thermal flow, i.e. 4 bipolar transistors - 4 electrical connection lines - not electrically isolated from silicon, so sensitive to RF disruptions	- sensitivity: 210 µV/K (per junction !) - Power free : no need of supply current - 2 electrical connection lines - electrically isolated from silicon: no RF disturbance - less sensitive to noise thanks to decoupling capacities *



Equivalent electrical schematic of Intel sensors made of 2x2 transistors to supress parasitic resistances



Equivalent electrical schematic of TES

* *Patent WO2012131183*

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STAND-ALONE µTES

- Develop TE technologies for materials and modules from

  TRL3 → TRL6

- Address **key technological challenges** (improve TE materials and devices performance)

TRANSFER

HBOB Sensors

- Scale-up TE technology from

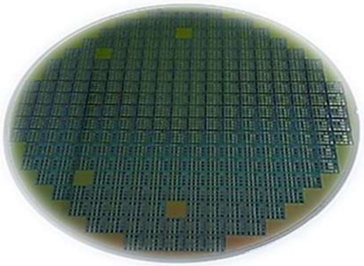
  TRL6 → TRL9

- Address **market needs**
- Main applications: **bulk TE generators (HotBlock OnBoard) and thin films thermal flow sensors (HBOB Sensors)**

- **Strategy**
  - Thermal management from packaged independent sensors (first manufacturing of such sensors) *
  - µTES developed in microelectronic technology at industrial scale:
    - manufacturing process based on 8 inches substrates
    - standard packaging from microelectronic

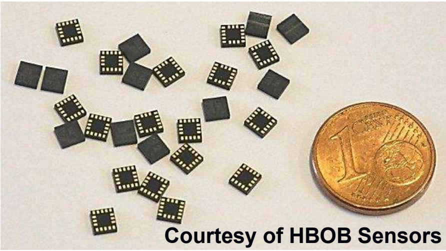
- **Main technological steps**

- 1 - Wafers manufacturing	- 2 - Chips manufacturing	- 3 - Chips packaging



Full wafer µTES manufacturing

Chip after slimming and cutting steps

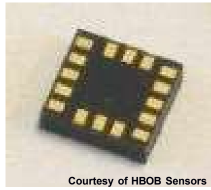


Chips after packaging

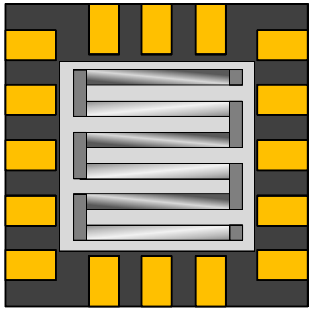
** Patent EP3035017*
Patent EP3035018

STAND-ALONE µTES

- **Stand-alone µTES chips design**

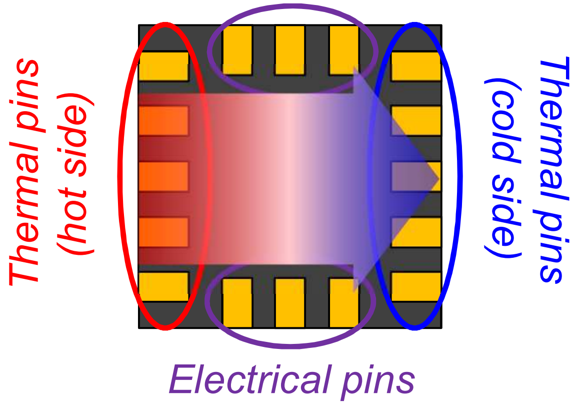


- Chips packaged from standard microelectronic packaging
  Size: 3 x 3,2 x 0,8 mm^3



- Design and manufacturing of several sensors geometries inside the package to propose different performances range

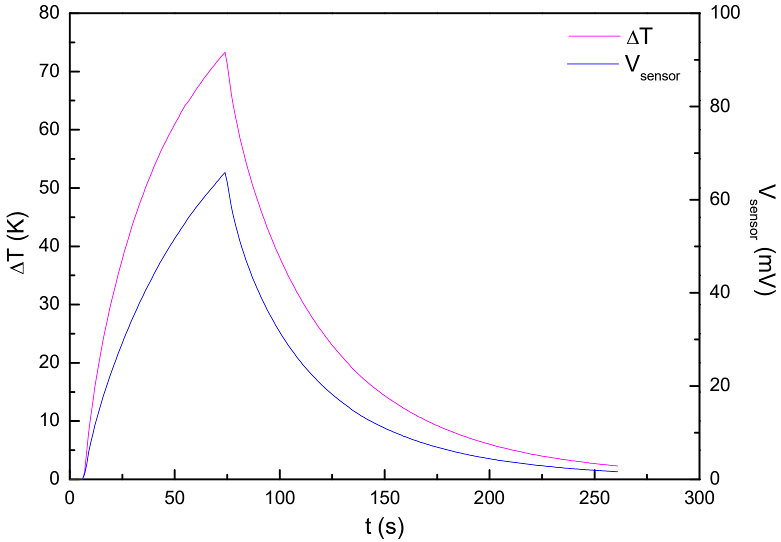
- Pins of packaging used for thermal and electrical connections



- **Chips characteristics**

→ TE materials: doped Si-based materials

Evolution of V_{sensor} (Type 1) and ΔT as a function of time

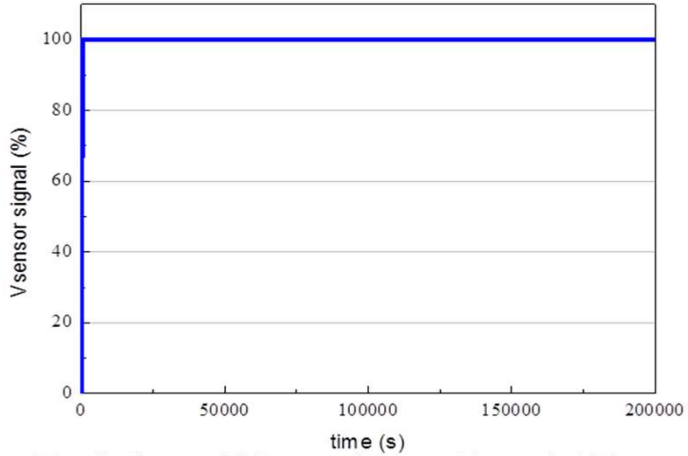


→ Very high µTES signal quality

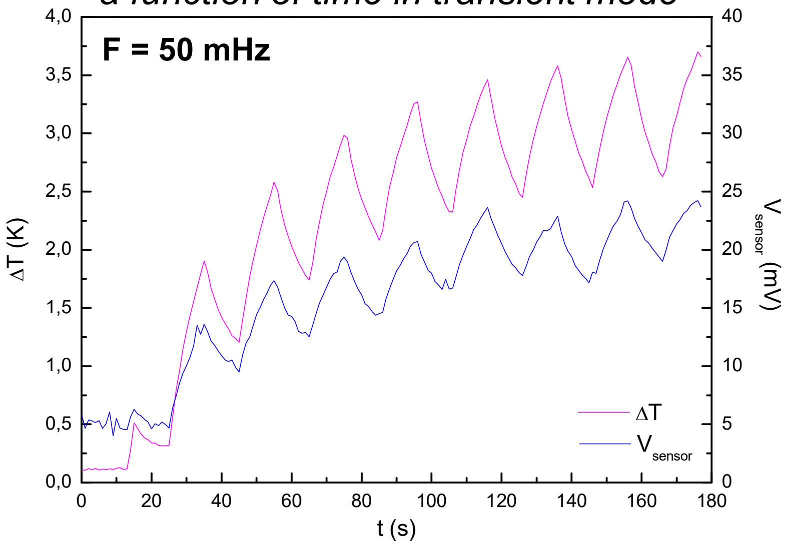
→ Very good µTES sensitivity stability

→ Very good µTES reactivity

Evolution of sensitivity (Type 2) with a continuous thermal flow (T_{hot} = 110 °C) for 2 days



Evolution of V_{sensor} (Type 3) and ΔT as a function of time in transient mode



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ON-INTERPOSER µTES

STREAMS
Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

- **H2020 ICT STREAMS project (2016-2019)**

  → Development of a generic SMART, ADAPTABLE and EMBEDDED active cooling thermal management solution, to keep nano-electronic devices and systems performances at their best (http://project-streams.eu)

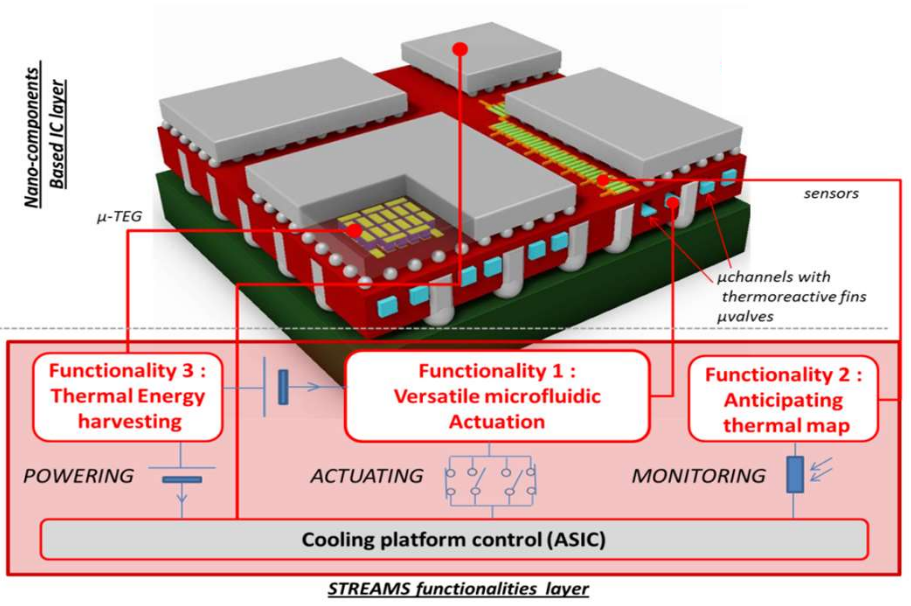
- **Development of three advanced functionalities and co-integration on Si-based interposer**

→ Functionality 1: Versatile microfluidic actuation, to manage liquid cooling of varying thermal scenarios in an energy efficient way

→ Functionality 2: Anticipating thermal map, to enable the real-time spatial control of the thermal state of dies → µTES technology

→ Functionality 3: Thermal energy harvesting to provide sufficient energy to power the developed active cooling thermal management solutions → µTEG technology

STREAMS – Generic autonomously-smart cooling platform



ON-INTERPOSER µTES

- **Strategy**
  - Thermal management from unpackaged integrated heat flux sensors at the interposer level to anticipate thermal map variation *
  - µTES developed in microelectronic technology

- **On-interposer µTES concept**
  - Several µTES processed directly on interposer for thermal mapping, located near hot chips
  - µTES connected to a read-out interface (ASIC) for signal management
  - Planar µTES with specific optimized design

** Patent WO2013017750*

ON-INTERPOSER µTES

- **µTES integration on interposer**

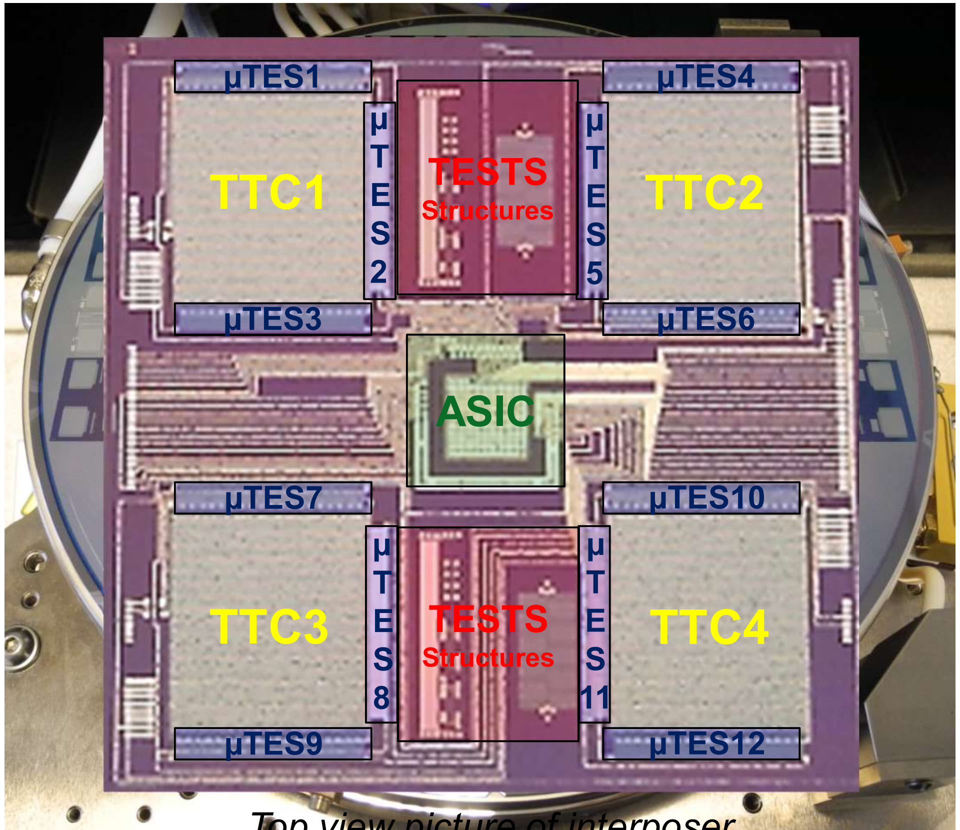
- Technology developed on 8 inches Si substrate
- Silicon-based interposer integrating:

4 Thermal Tests Chips (TTC)
→ designed to allow thermal studies with a strategy of versatile heaters and hotspots in real dice

12 µTES
→ located around each TTC for thermal mapping

1 Application-Specific Integrated Circuit (ASIC)
→ µTES read-out interface for signals management

2 Tests structures areas
→ structures to control TE materials and process flow

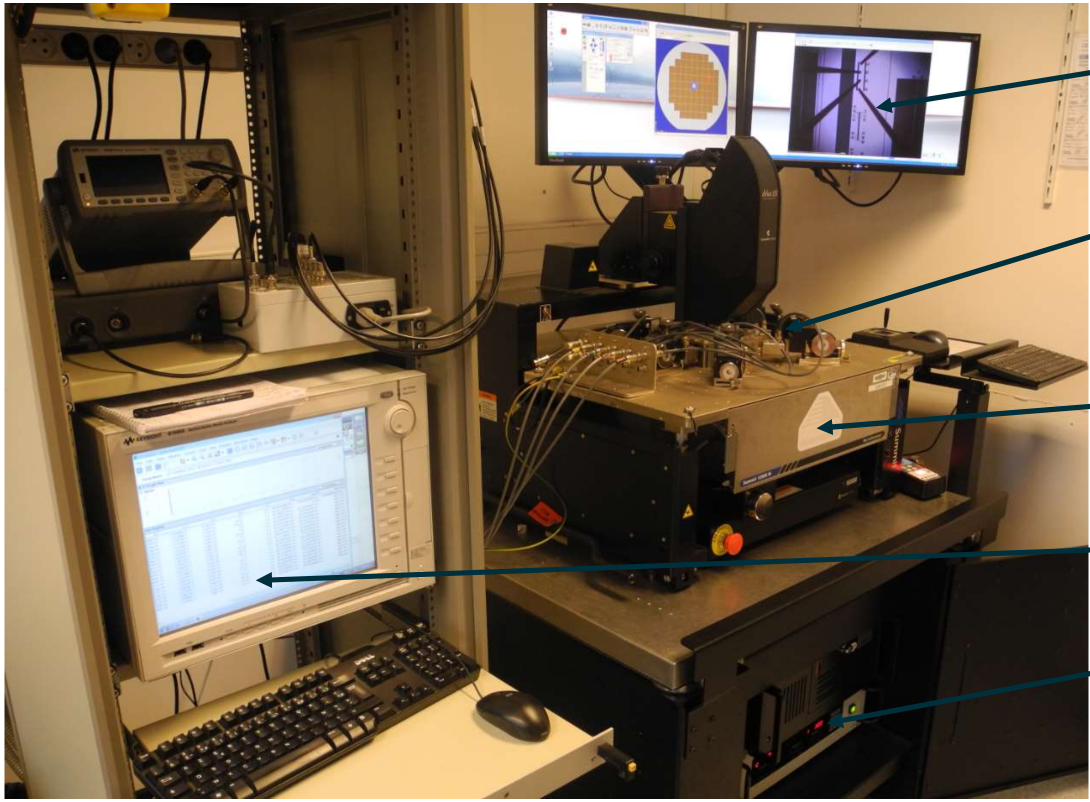


Top view picture of interposer
Picture of a processed wafer

ON-INTERPOSER µTES

STREAMS
Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

- **Characterization tool**



View of tested patterns

Probes connecting patterns and analyzer

Wafer inside a thermal controlled micro-chamber

Analyzer

Temperature control

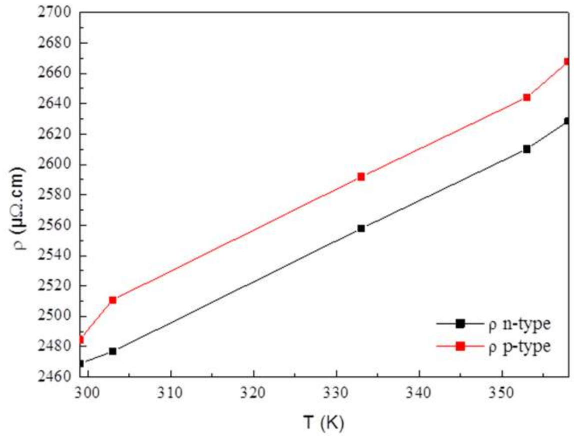
Picture of the probe station used for the µTES characterization

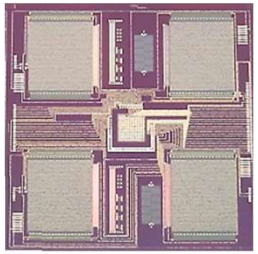
ON-INTERPOSER µTES

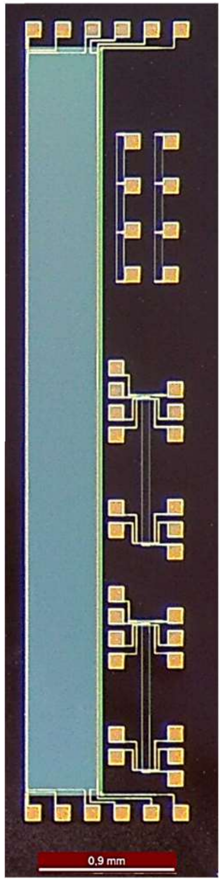
- **TE materials characterization**

- TE materials: doped poly-SiGe
- Measurement of TE materials electrical resistivity ρ and Seebeck coefficient S
  → ρ measured by 4 probes method
  → S measured by dedicated structures with heater and thermal controlled metallic lines

Evolution of electrical resistivity as a function of temperature







TE materials properties at 300 K

TE materials	ρ (Ω.m)	S (µV/K)	PF (W/m/K²)
n-type SiGe	$2,4.10^{-5}$	-200	$1,7.10^{-3}$
p-type SiGe	$2,5.10^{-5}$	+160	1.10^{-3}

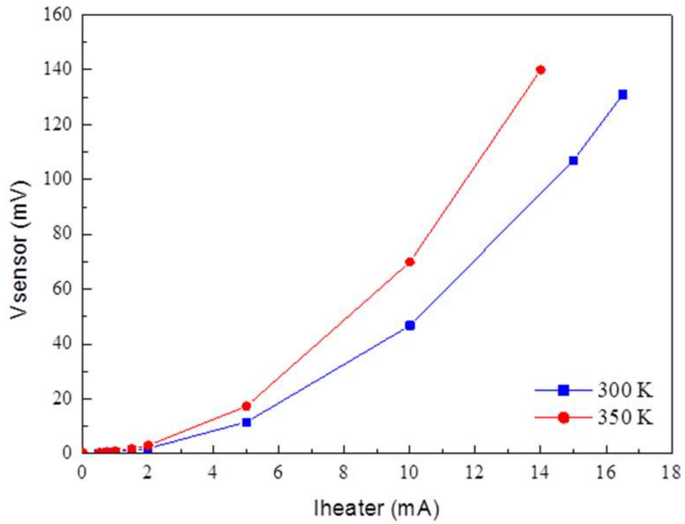
→ coherent TE properties for poly-SiGe materials

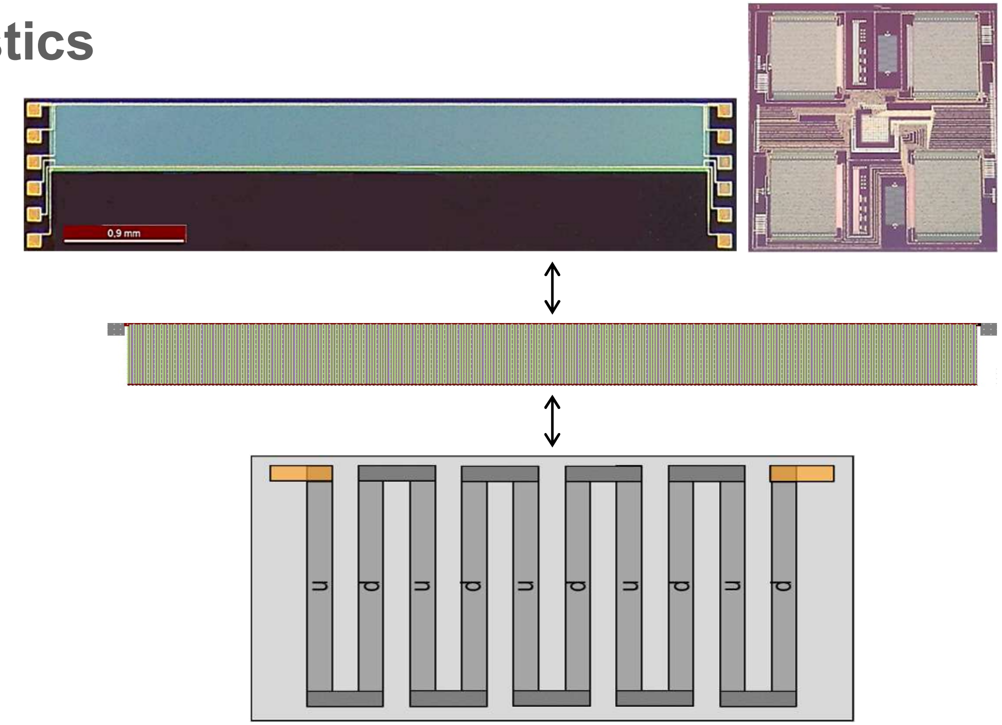
ON-INTERPOSER µTES

- **µTES design and characteristics**

  - Standard 2D planar structure
  - µTES size: 5 x 0,5 mm²
  - Junctions number: 315

Evolution of µTES voltage as a function of heater current





On-interposer µTES properties

On-interposer µTES	300 K	350 K
Electrical resistance (kΩ)	960	1007
Sensitivity (mV/K)	110	130

→ coherent µTES properties compared to TE materials properties

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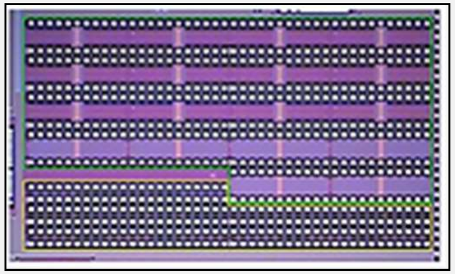
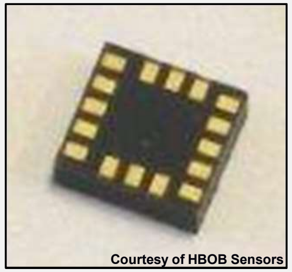
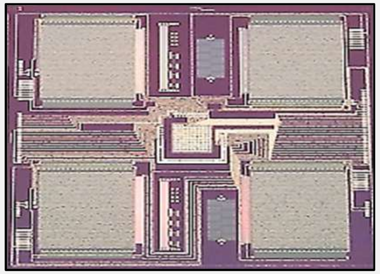
CONCLUSIONS

- **Main characteristics of µTES technologies**

Technology	“in-IC”	“stand-alone”	“on-interposer”
			
TE materials	Doped Si (= transistor’s gate)	Doped Si-based materials	Doped SiGe
Area	0,012 mm²	9,6 mm²	2,5 mm²
Sensitivity	80 mV/K	10 mV/K	110 mV/K
Electrical resistance	50 MΩ	Confidential	960 kΩ
Thermal resistance	9 K/W	Confidential	5 K/W
Response time	≈ 10 ms	≈ 1 s	≈ 300 ms

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PERSPECTIVES

- **In-IC µTES technology**
  - µTES development and integration for CMOS technology (Si-based) well mastered
  - Development of new in-IC µTES for power components technology (GaN-based) in progress

- **Stand-alone µTES technology**
  - First manufacturing of packaged thermal sensors
  - Technology transferred to HBOB Sensors
  - Development a new stand-alone technology based on optimized substrates

- **On-interposer µTES technology**
  - Technology characterization still in progress
  - Characterization of µTES with ASIC has to be done and thermal mapping concept has to be validated

ACKNOWLEDGEMENTS

- **EUROPEAN UNION**

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STREAMS

Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

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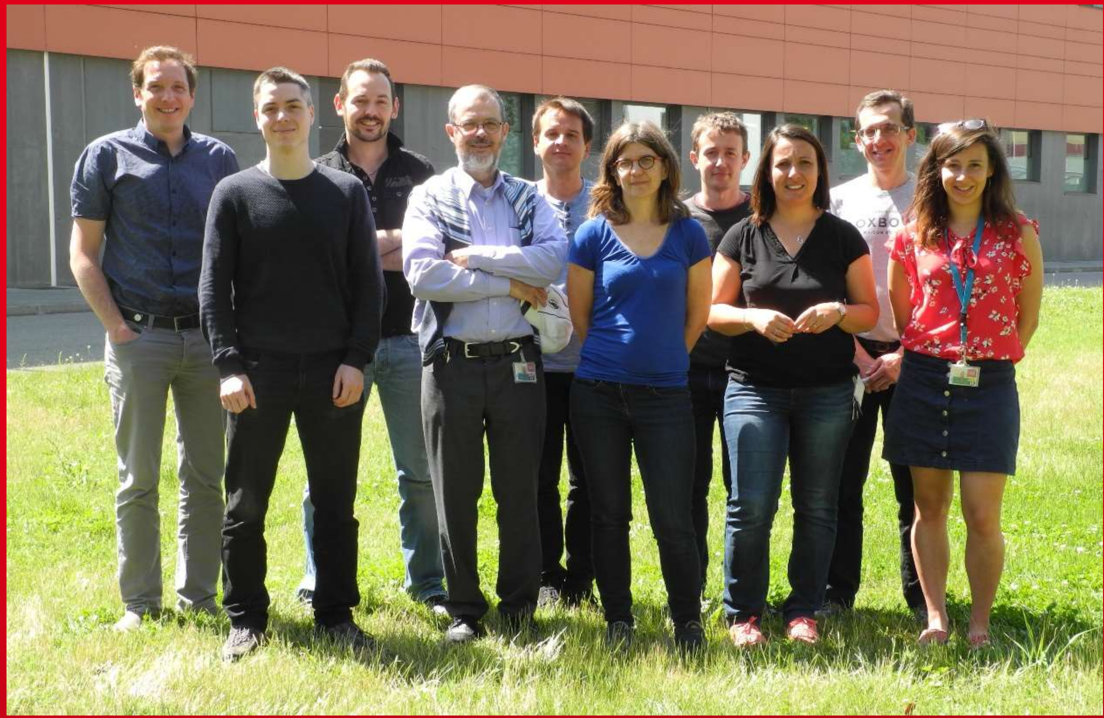

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