STREAMS

Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

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Smart Technologies for eneRgy Efficient Active cooling in advanced Microelectronic Systems

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D3.5

ROI / ASIC and Electrical Characterization ROI

WP	3	Anticipating Thermal Map
Task	3.5	Anticipating thermal map proof of concept

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Authors	Proofreader
M. Keller & D. Wendler	G. Savelli

[1] Dissemination level: **PU** = Public, **PP** = Restricted to other program participants (including the Commission services), **RE** = Restricted to a group specified by the consortium (including the JU), **CO** = Confidential, only for members of the consortium (including the Commission services).

[2] Nature of the deliverable: **R** = Report, **D** = Demonstrator, **O** = Other.

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[3] Creation, modification, final version for evaluation, revised version following evaluation, final.

Deliverable abstract

This report summarizes the electrical characterization of the read-out interface (ROI) for the micro-thermo-electric flow sensors (µTESs) and temperature sensors (TSs). For this purpose, a versatile modular evaluation board was designed and implemented which can also be used for the electrical characterization of the power management unit as well as for the characterization of the ASIC plus the µTESs / TSs and for the final demonstrator.

Based on the outcome of the electrical characterization of the ROI, it is concluded that all specifications are met, i.e., the ROI is ready to be used for performing measurements with the µTESs and TSs. A signal-to-noise-and-distortion ratio (SNDR) and thus an effective resolution of 9.3 bits were measured in a signal bandwidth of 125Hz. The measured worst-case power consumption, which is drawn from a 3.3V supply voltage, results in 0.94mW. An autonomous powering of the ROI is thus considered feasible with a power budget of 6mW which is expected to be harvested by the µTEGs.

Table of content

1 – Introduction

In task 3.5, the electrical characterization of the fabricated integrated read-out interface (ROI) designed in task 3.4 is performed. The ROI monitors and digitizes the thermal flow and the temperature of four thermal test chips (TTCs) by means of twelve micro-thermoelectric flow sensors (µTESs) developed by our partner CEA and four temperature sensors (TSs) provided by our partner STMicroelectronics.

The tape-out of the ROI was performed in April 2017 while the application-specific integrated circuits (ASICs) shown in Figure 1, consisting of the ROI and the power management unit (PMU), were delivered in August 2017.

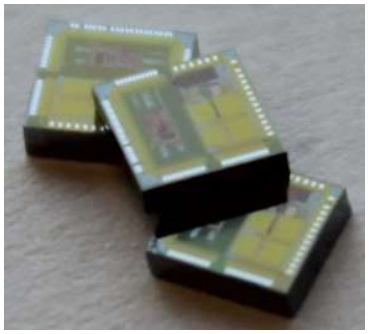


Figure 1: Fabricated ASICs.

In close cooperation with all partners, an evaluation board (EB) was implemented as a printed circuit board (PCB) in order to perform the electrical characterization of the ASICs. Its design is presented in Chapter 2 whereas the measurement results are summarized and discussed in Chapter 3.

2 – Design of the Evaluation Board

Considering that an EB is required not only for the electrical characterization of the ROI but also for the characterization of the power management unit as well as the ASIC plus µTESs / TSs and for the final demonstrator, much effort and thus time was spent on its design. Ultimately, the approach will pay off since the EB can be applied to all scenarios. The EB is implemented as a modular system that is presented in section 2.1. Details on the specific parts for the electrical characterization of the ROI are given in section 2.2.

2.1 Evaluation Board – Overview of the Modular System

As illustrated in Figure 2, the EB is implemented as a PCB to which auxiliary PCBs and a microcontroller can be connected by means of sockets and pin strips. A modular system is thus implemented which provides a high grade of adaptability and options, e.g., the electrical characterization of an arbitrary number of ASICs by means of a single EB. The main components of the EB are:

- an auxiliary PCB *interposer* which has a milled area for implementing the microfluidic channels using PDMS as substrate. On top of the substrate, the four TTCs and the twelve µTESs will be implemented whereas the micro-thermoelectric generators (µTEGs) will be implemented between the substrate and the TTCs.

- an auxiliary PCB *ASIC* on which the ASIC consisting of the ROI and PMU is mounted.

- an auxiliary PCB *FPGA* which is used for the electrical characterization of the ROI and the PMU. The FPGA allows for generating test signals, capturing data, and connecting the EB to a PC by means of a universal serial bus (USB).

- a microcontroller which can be connected to the EB by means of a pin strip. It will be used for the closed-loop control of the microfluidic system.

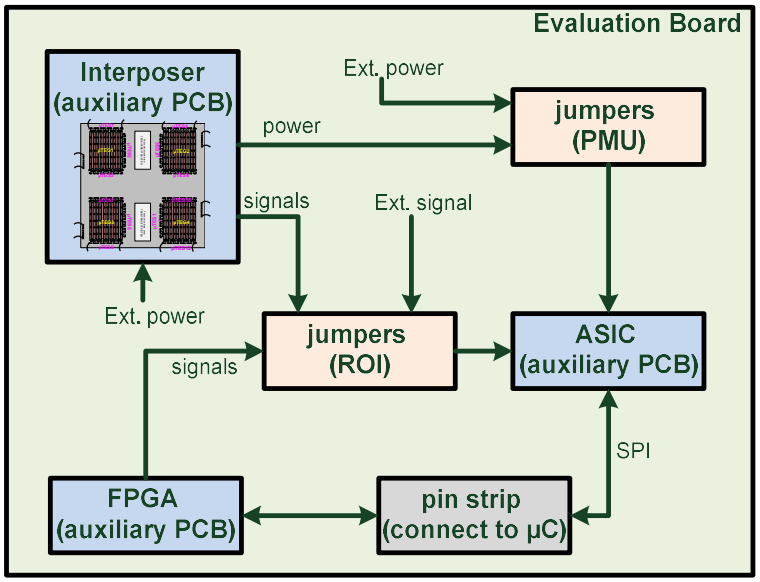


Figure 2: System overview of the modular evaluation board.

- jumpers that allow selecting the signals connected to the ROI, i.e., test signals generated by the FPGA / external signal generator or the signals of the device under test, i.e., the signals of µTESs and TSs of the TTCs. Moreover, by means of a jumper, it can also be selected whether the ASIC is powered by the µTEGs or an external power source.

2.2 Evaluation Board – Read-out Interface Specific Part

The block diagram of the read-out interface specific part of the EB is shown in Figure 3.

The auxiliary PCB *FPGA* is implemented using an XEM6010-LX150 board of Opal Kelly which has a Spartan-6 FPGA. It can be connected to and thus be programmed via a PC by means of its USB and application programming interface (API).

The FPGA controls two digital-to-analog converters (DACs) in order to emulate the signals of the µTESs and TSs. A generation and application of further signal waveforms, amplitudes, and frequencies by the FPGA or an external signal generator is feasible. Moreover, the USB and the serial-peripheral interface (SPI) allow configuring the ROI and transmitting data from or to a PC. Overall, test automation and evaluation of the results can easily be performed due to the FPGA.

As summarized in D3.2, various internal analog and digital signals of the ROI can be monitored. However, analog signals of the ROI must be digitized before being applied to the FPGA. This task is performed by an ADC whereas the internal signal of the ROI applied to the ADC is selected by the multiplexer *MUX*.

Finally, two low drop-out regulators (LDOs) were implemented in order to provide the option of powering the analog and digital part of the ROI by external voltage generators instead of the µTEGs. Thus, the ROI can be used in case the µTEGs and / or the PMU do not harvest enough power or are inoperable. Whether the ROI is powered by the µTEGs / PMU or the external voltage generators can be selected by means of a jumper.

The fabricated EB and the auxiliary PCBs are shown in Figure 4. The EB was implemented as a four-layer PCB with an area of 27.8cm x 11.7cm. The auxiliary PCBs *ASIC* and *interposer* were implemented using single-layer PCBs with areas of 3.8cm x 3.8cm and 8.5cm x 5.5cm, respectively. The area of the Opal Kelly LX150 board results in 7.5cm x 5.0cm.

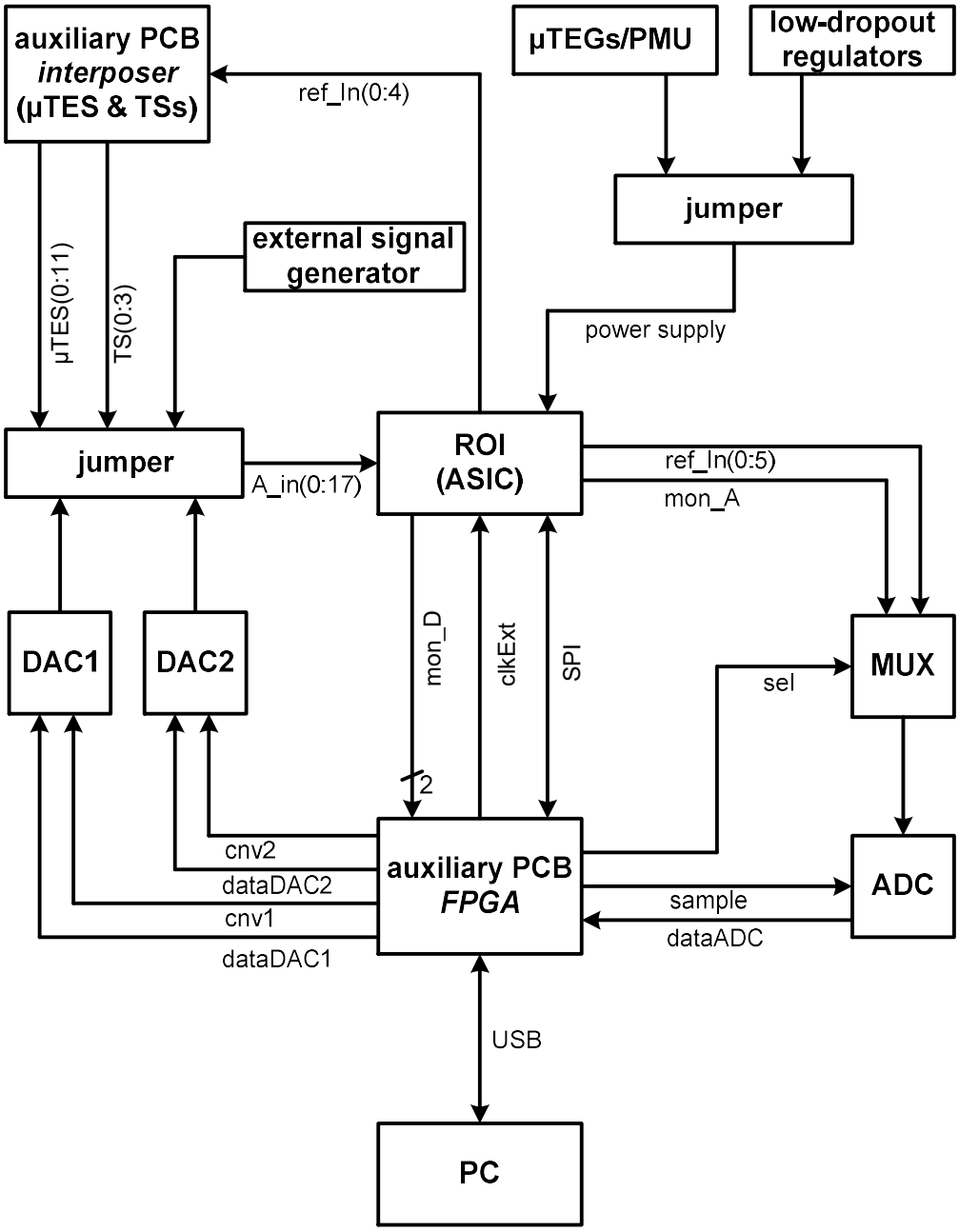
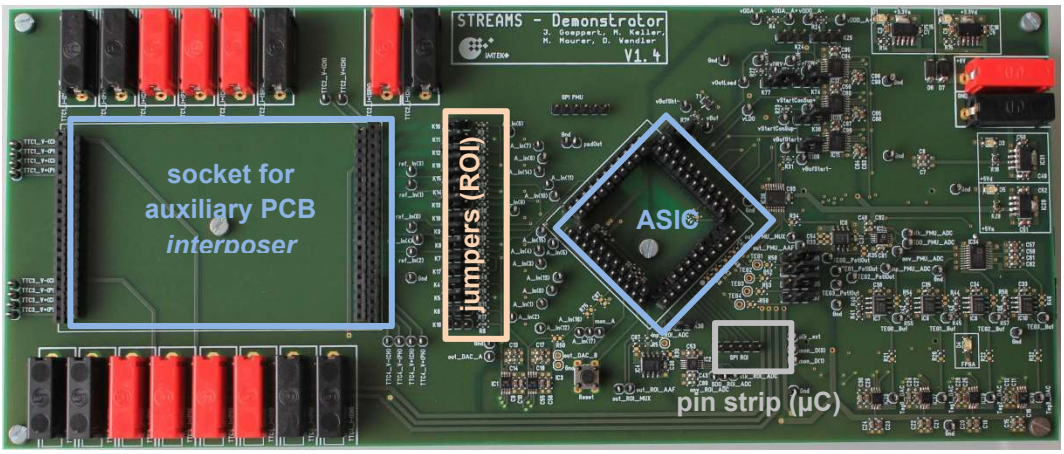
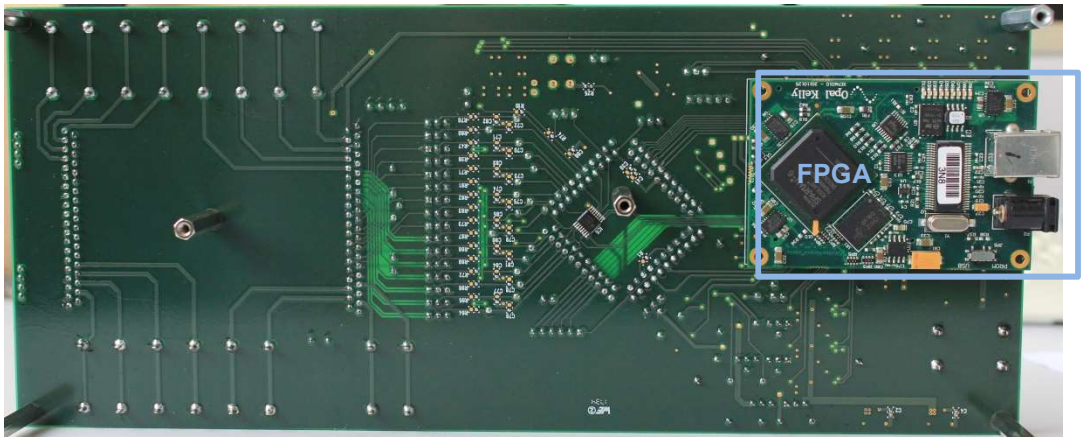


Figure 3: Block diagram of the read-out interface specific part of the evaluation board.

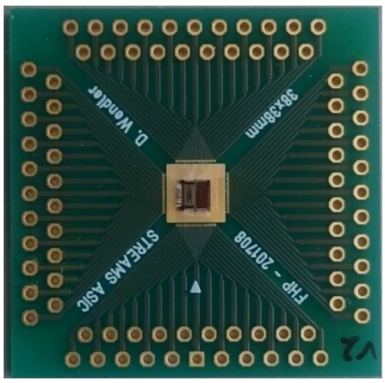


a) front side of the evaluation board

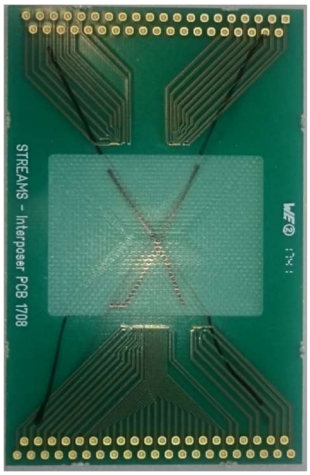


b) backside of the evaluation board

c) auxiliary PCB *FPGA*



d) auxiliary PCB *ASIC*



e) auxiliary PCB *interposer*

Figure 4: Fabricated modular evaluation board (four-layer printed circuited board).

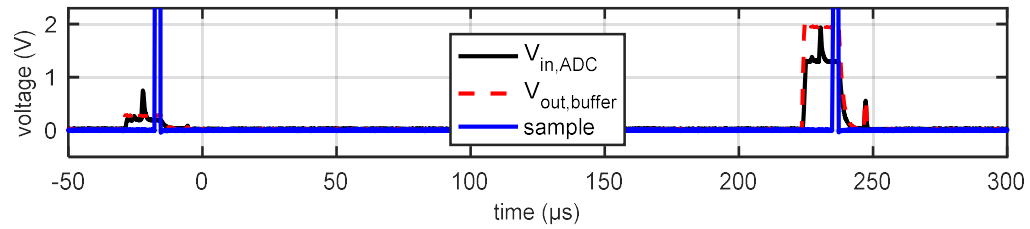
3 – Measurement Results

3.1 Settling Behavior

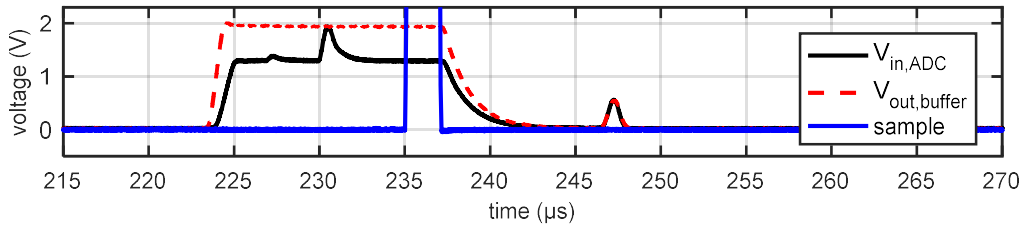
As discussed in deliverable D3.2, a voltage step of 1.65V, which may occur when switching from one channel to the next channel due to the multiplexing approach, depicts the worst case for the settling behavior. In order to emulate this case and thus to measure the step response of the ROI, voltages of 0.25V and 1.9V were respectively applied to two neighboring channels of the ROI by means of DAC1 and DAC2, which in turn are controlled by the FPGA (see Figure 3). Note that the minimum input voltage of the ROI equals 0.25V in order to see to it that its amplifier operates in the linear region of its transfer characteristic. Consequently, the gain of the amplifier of the ROI was set equal to 4/6 in order to match the signal swing of 1.9V to the 1.25V full-scale range of the successive approximation register analog-to-digital converter (SAR ADC). The worst-case output resistance of the µTESs (nanostructured QDSL, geometry G1) was emulated by implementing a 4.02MΩ resistor in front of each input pad of the ROI.

The measurement results of the settling behavior of the signals $V_{out,buffer}$ (output signal of the buffer) and $V_{in,ADC}$ (input signal of the SAR ADC) are shown in Figure 5. The measurements were performed by applying the signals successively to the analog monitoring pin *mon_A* whereas the digital signal *sample* of the SAR ADC was monitored by the digital monitoring pin *mon_D* (see Figure 3).

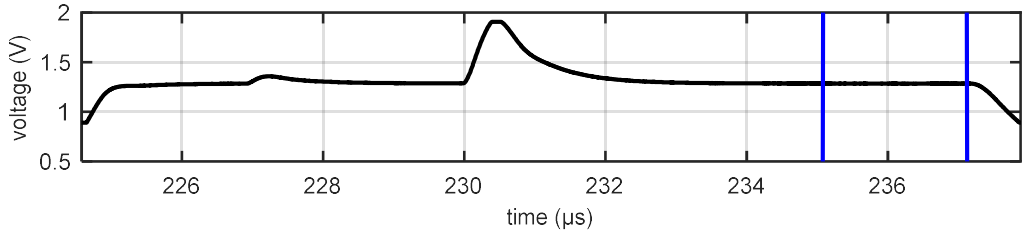
The measurement cycle of two neighboring channels is shown in Figure 5.a. Considering the signal $V_{out,buffer}$, it can be seen that 0.25V and 1.9V were applied to the ROI as discussed above. The zoom of the period 215µs to 270µs (Figure 5.b) shows that the signal $V_{in,ADC}$ equals the signal $V_{out,buffer}$ multiplied by 2/3. Finally, the zoom of the period 224µs to 238µs (Figure 5.c) shows that the signal $V_{in,ADC}$ is well settled when the sampling and thus the analog-to-digital (A/D) conversion is performed.



a) two sampling periods



b) zoom of a) into the period 215µs to 270µs



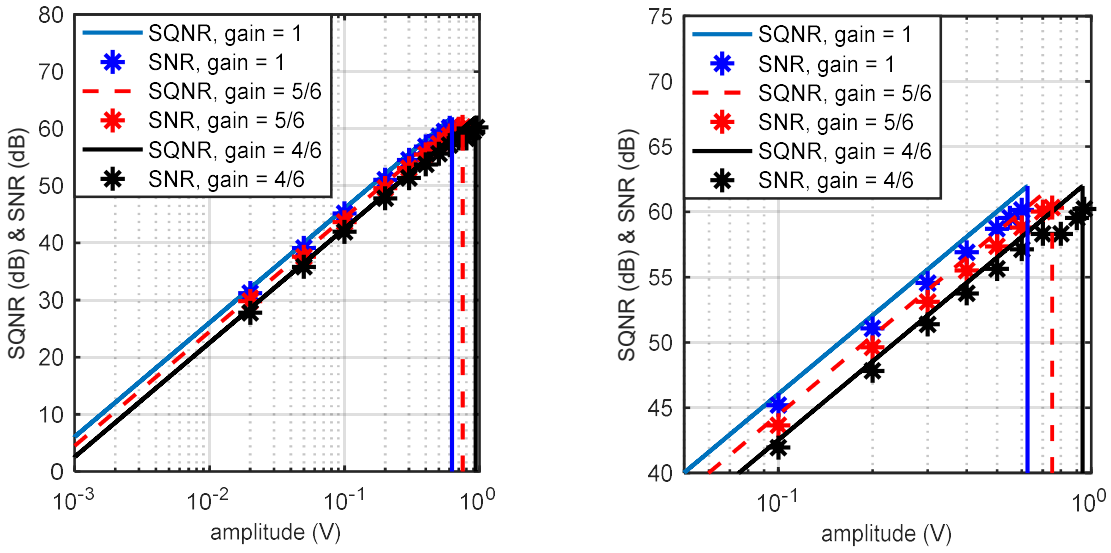
c) zoom of a) and b) into the period 224µs to 238µs

Figure 5: Settling behavior of the read-out interface.

3.2 Dynamic Performance – Resolution (signal-to-noise ratio & signal-to-noise-and-distortion ratio)

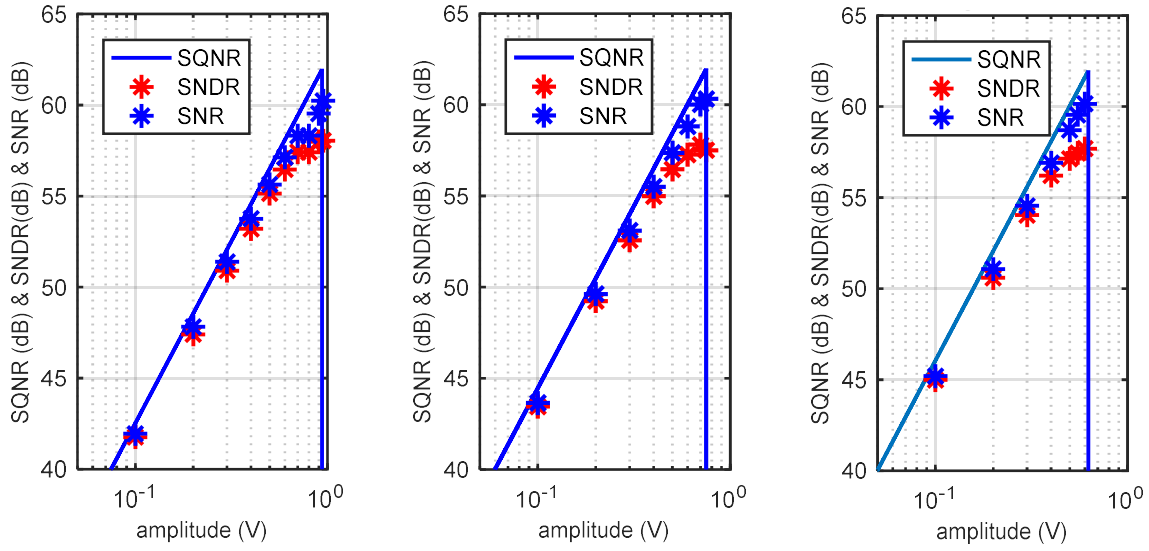
In Figure 6, the measurement results of the signal-to-noise ratio (SNR) and the calculated characteristic of the signal-to-quantization-noise-ratio (SQNR) of the ROI are shown. Note that the mean values of the measurements are given, i.e., the average of the measurements performed on the 16 channels. In doing so, a sinusoidal signal with a frequency of 1Hz was applied to the ROI, which was generated by an external signal generator. 2^{15} measurements were recorded per amplitude, gain setting, and channel, and applied to a fast Fourier transform in order to calculate the power spectral density (PSD). Based on the PSD, the power of the quantization noise and the noise-and-distortion were determined by integrating the respective PSD from 0Hz to the signal bandwidth of 125Hz, i.e., the sampling frequency results in 250Hz per channel due to the multiplexing approach.

The zoom of the amplitude range 50mV to 1V shown in Figure 6.b proves that the ROI achieves a resolution of 10 bit for all gain settings since the measured peak SNR is larger than 60dB.



a) full amplitude range **b) zoom of the amplitude range 50mV to 1V**

Figure 6: Calculated signal-to-quantization-noise ratio and measured signal-to-noise ratio.



a) gain setting = 4/6 **b) gain setting = 5/6** **b) gain setting = 1**

Figure 7: Calculated signal-to-quantization-noise ratio (SQNR), measured signal-to-noise-and-distortion ratio (SNDR), and measured signal-to-noise ratio (SNR) for all gain settings.

The averaged measurement results of the signal-to-noise-and-distortion ratio (SNDR) are shown in Figure 7, where also the calculated SQNR and measured SNR are shown again for reasons of comparison. Since the averaged peak SNDR results in 57.7dB, an effective resolution of 9.3 bits is achieved.

3.3 Static Performance – Integral & Differential Nonlinearity

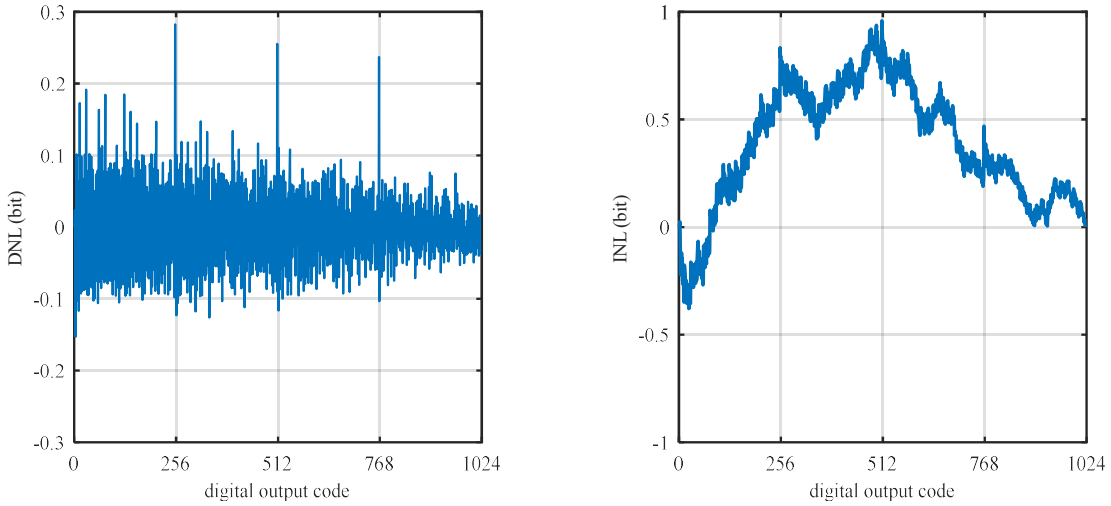
The static performance of any ADC is rated based on the differential nonlinearity (DNL) and integral nonlinearity (INL). Considering an ideal ADC, the step width between two adjacent output codes results in one least significant bit (LSB). The DNL is defined as the difference of each step width minus the ideal step width normalized to the LSB. The INL is defined as the difference of each transition point minus the ideal transition point of an ideal transfer characteristic defined by the straight line connecting the first and the last transition point. As for the DNL, the INL is normalized to the LSB.

The INL and DNL of the ROI were determined by applying the histogram method. Hence, a full scale sinusoidal signal of 1Hz generated by an external signal generator was applied to the ADC. For calculating DNL and INL with a confidence level $Z_{\alpha/2}$ by means of the histogram method, a certain number N of measurements are required according to

$$N = \pi 2^{n-1}\left(Z_{\alpha/2}\right)^2/\beta^2 \qquad (1)$$

where β is the resolution of the DNL / INL and n the resolution of the ADC in bits.

According to (1), one million measurements are required in order to determine the DNL and INL of a 10-bit ADC, i.e., n = 10, with a confidence level of 99%, i.e., $Z_{\alpha/2}$ = 2.58, and a resolution β = 0.1bit. Hence, 2^{20} measurements were recorded. The resulting DNL and INL are shown in Figure 8. The DNL is smaller than ±0.3 bits over all codes. As expected, the maxima occur at the codes 256, 512, and 768 due to the binary weighted implementation of the SAR ADC. The INL is smaller than one LSB and shows a maximum in the middle of its transfer characteristic at code 512 which matches well with the measured effective resolution of 9.3 bits, i.e., the SNDR, according to 3.3.



a) DNL **b) INL**

Figure 8: Measured differential (DNL) and integral nonlinearity (INL) of the read-out interface

3.4 Power Consumption

For the evaluation of the average power consumption, series resistors R_s of 100Ω were implemented in the digital and analog power supply line of the evaluation board. By means of measuring the voltage drop $V_s(t)$ over the resistor R_s, the average digital and analog power consumption P_c are calculated according to

$$P_C = \frac{V_{CC}}{t_1 - t_0} \int_{t_0}^{t_1} \frac{V_s(t)}{R_s} dt \quad (2)$$

where V_{CC} is 3.3V for both the digital or analog supply voltage, t_0 the start time of the conversion cycle, and t_1 to the stop time point of the conversion cycle.

The average power consumption per conversion was determined over one conversion cycle which consists of 220 clock cycles for the settling of the signal $V_{in,buffer}$ plus 15 clock cycles for the settling of the signal $V_{in,ADC}$ plus 12 clock cycles for performing the A/D conversion by the SAR ADC.

Enabling the generation of the reference voltage V_{ref} = 250mV by the ROI as will be performed when converting the signals of the µTESs, the measured power consumption P_C results in 0.94mW of which 0.66mW and 0.28mW are consumed by the analog and digital part, respectively. Disabling the generation of V_{ref} as will be performed when converting the signals of the TSs, the measured power consumption P_C results in 0.46mW (0.23mW analog, 0.23mW digital). Thus, an autonomous powering of the ROI is considered feasible with a power budget of 6mW which is expected to be harvested by the µTEGs.

4 – Conclusion & Next Steps

Based on the outcome of the electrical characterization of the ROI, it is concluded that the ROI is ready to be used for performing measurements with the µTESs and TSs. From a current perspective, a redesign needs not be performed. The date of the joint measurements will be organized with our partner CEA in August / September 2018.