Embedded Thermal Energy Harvesting – Challenges & Opportunities

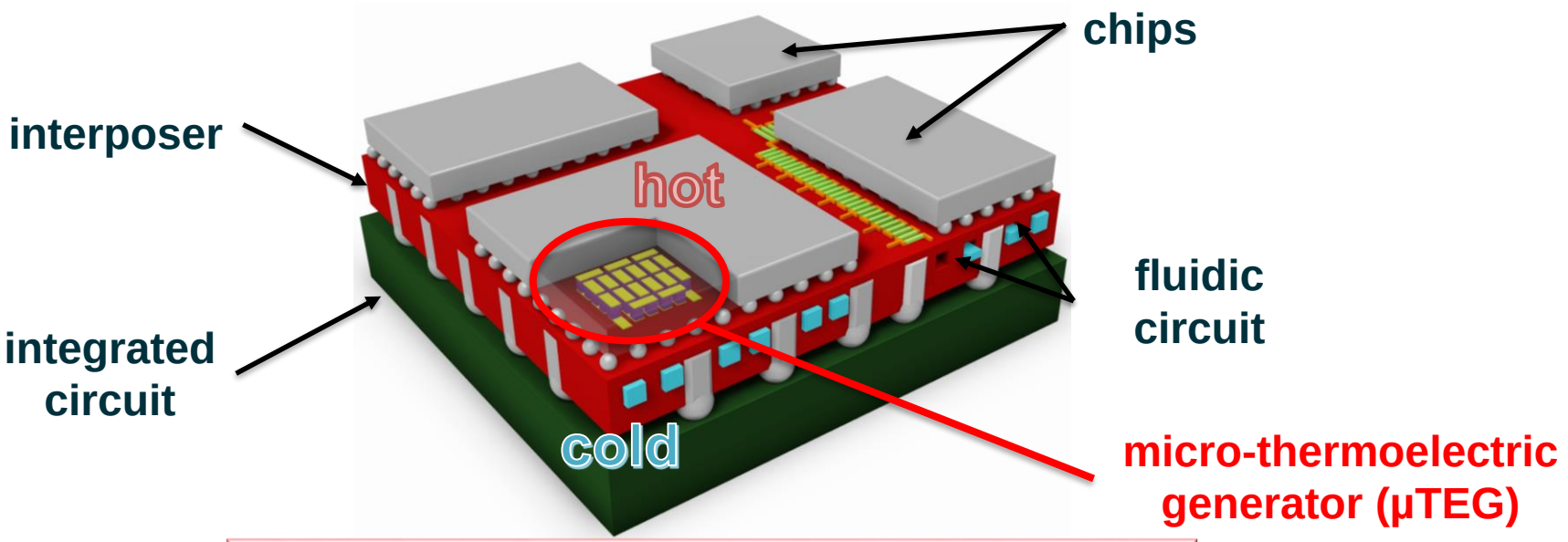
M. Keller, J. Goeppert, Y. Manoli, G. Savelli, J.-P. Colonna, P. Faucherand, L.-M., Collin, L. Fréchette

STREAMS

Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

STREAMS – Objectives

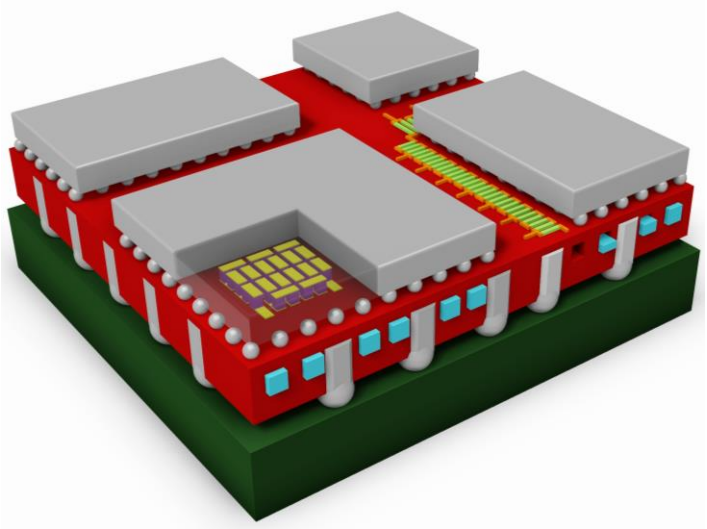
- Implementation of a **self-adaptive** microfluidic cooling system
- Minimization of the **pumping power** dedicated to coolant
- Enhancement of the surface **temperature uniformity** of the interposer



Investigate the opportunity to perform thermal energy harvesting!

Outline

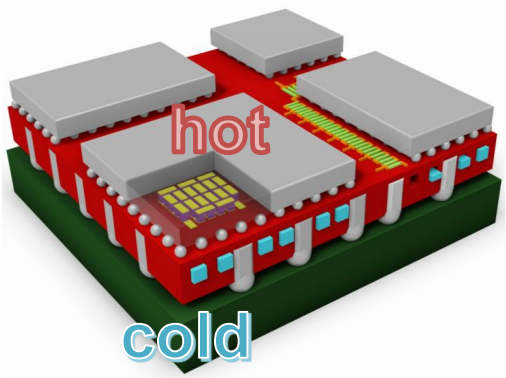
- **µTEG – Design & Implementation**
- Integrated Digital Circuit Design @ Ultra-low Supply Voltages
- Conclusion



µTEG - Objectives

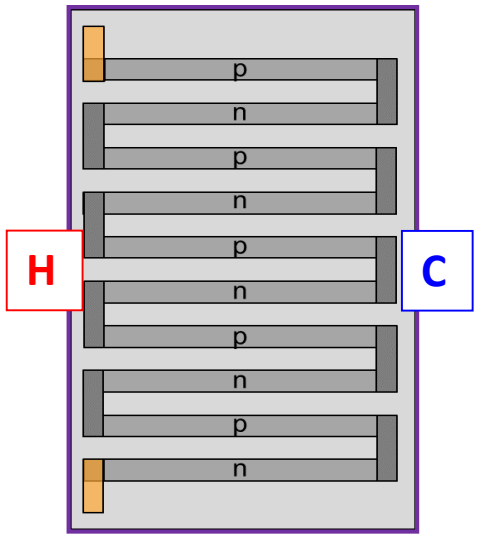
1. Design & implement a 2.5D µTEG which
   - harvests power of several mWs
   - consists of materials that can be processed using standard fabrication steps of integrated circuits

2. Integrate four µTEGs into a demonstrator which consists of
   - four ASICs (hot source) cooled by means of
   - fluidic microchannels (cold source)



µTEG – 2.5D Architecture

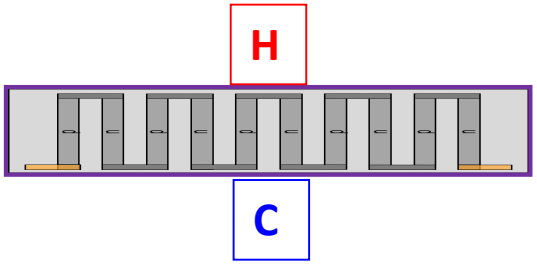
2D architecture (planar)



top view

- lines consisting of either n- or p-type materials
- in-plane thermal & electrical flow

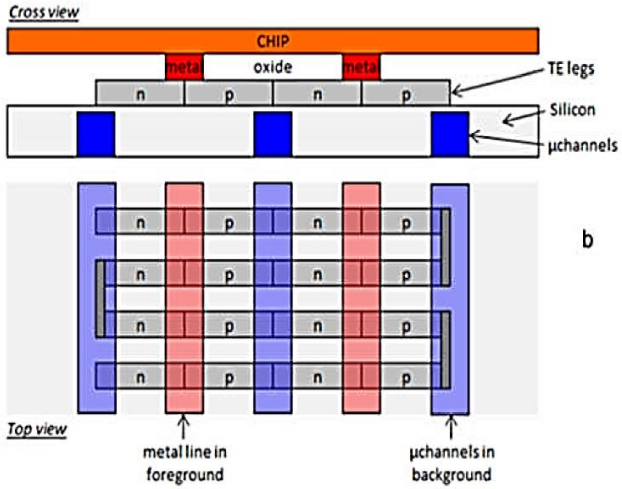
3D architecture (cross-plane)



cross-sectional view

- legs consisting of either n- or p-type materials
- out-of-plane thermal & electrical flow

2.5D architecture (combined)



cross-sectional & top view

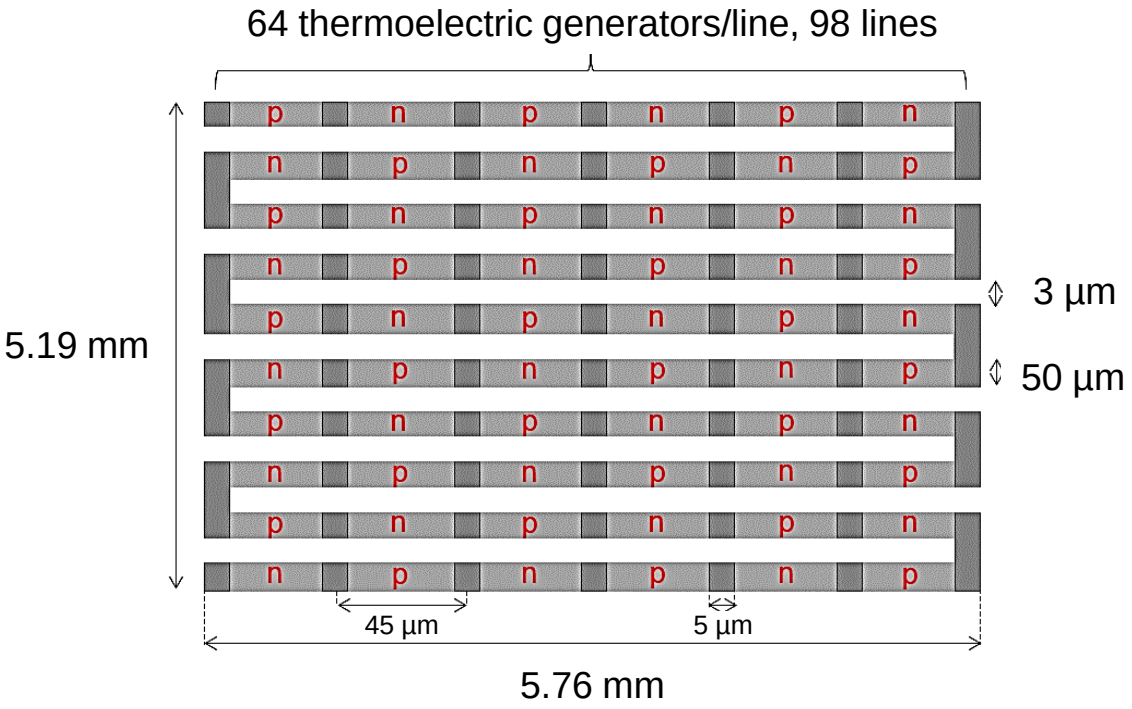
- lines consisting of n- & p-type segments
- thermal flow: out-of-plane
- electrical flow: in-plane

Design µTEG – Layout

Design objective: Harvest > 1mW

→ Maximize number of thermo-elements on the given area

Design & simulation: in-house software & COMSOL



Configuration of the µTEG

(4x lines in series) ||

(18 blocks parallel, each block

5x lines in series) ||

(4x lines in series)

Design µTEG – Materials

Design objective: Use materials that can be processed using standard fabrication steps of integrated circuits!

→ polycrystalline SiGe and quantum dots super lattices (QDSL)

		electrical resistivity ρ (Ωµm)	Seebeck coefficient S (µV/K)
SiGe	n-type	34	-185
	p-type	30	+142
QDSL	n-type	95	-268
	p-type	160	+253

Objective: Harvest > 1mW/µTEG

$$P = 1\text{mW} = \frac{1}{R_{\mu TEG}}\left(\frac{V_{OC}}{2}\right)^2 \approx \frac{1}{\frac{320}{18}\rho_{TE}\frac{l_{TE}}{t_{TE}w_{TE}}}\left(\frac{320 * V_{TE}}{2}\right)^2$$

minimum voltage V_{TE} per thermo-element

$$1\text{mW} = \frac{1}{\frac{1}{18}\frac{(30+34)\Omega\mu\text{m}}{2}\frac{100\mu\text{m}}{2\mu\text{m} * 50\mu\text{m}}}\frac{320}{4}V_{TE}^2 \rightarrow \boldsymbol{V_{TE} \approx 4.71\,mV}$$

required minimum temperature drop ΔT

$$V_{TE} = S * \Delta T \rightarrow \boldsymbol{\Delta T \approx 13.3°C}$$

Notes

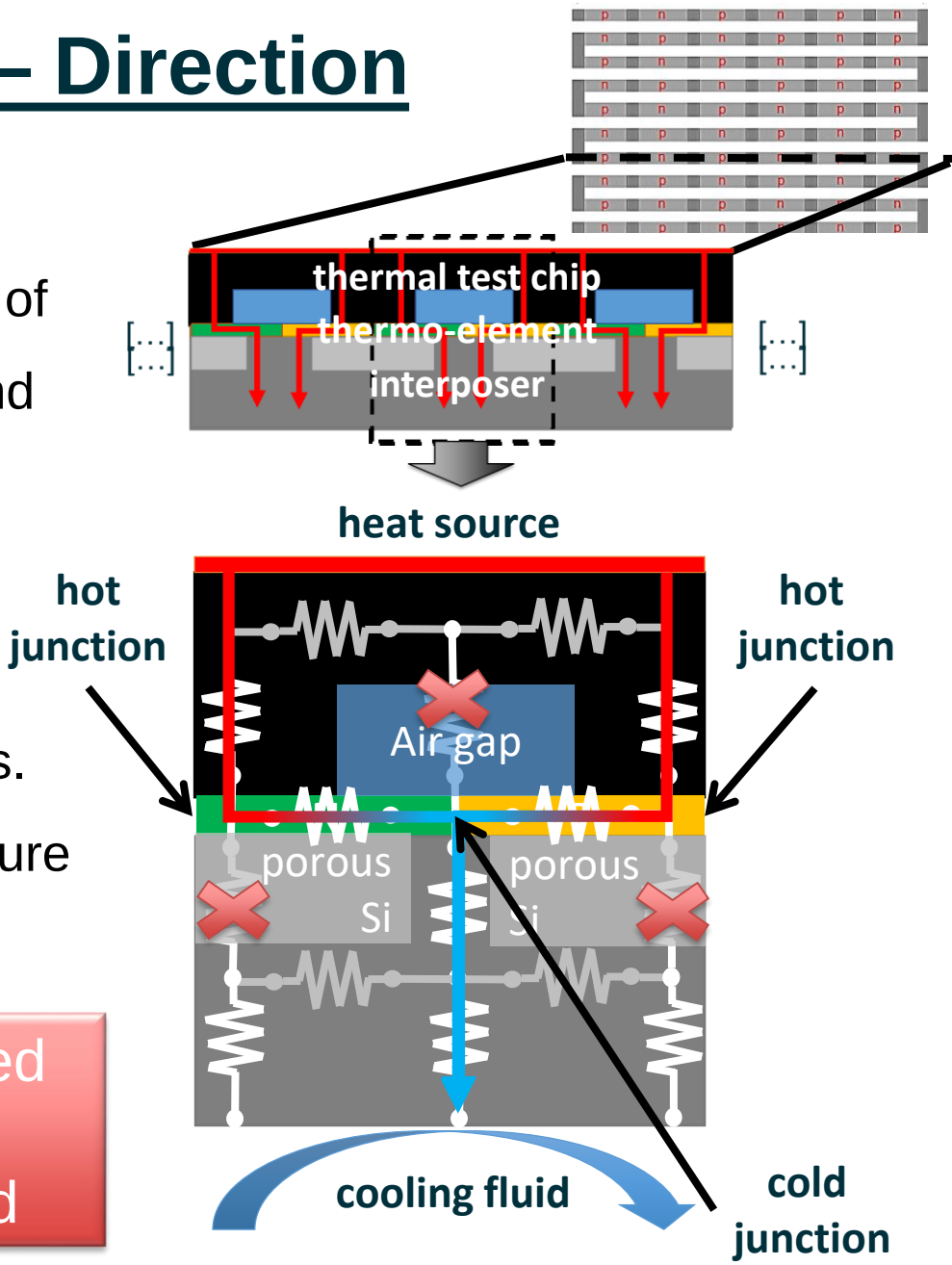
- parameters given on previous slides
- results for QDSL: 9.4mV / 18°C

Design µTEG – Direction Heat Flow

Define the hot & cold junction of each thermo-element (TE) and maximize its temperature gradient!

Air gaps define cold junctions. Porous Si maximizes temperature gradient across TE.

Vertical heat flow converted into horizontal heat flow
→ planar TE can be used



Design µTEG – Energy Harvesting vs. Cooling Efficiency

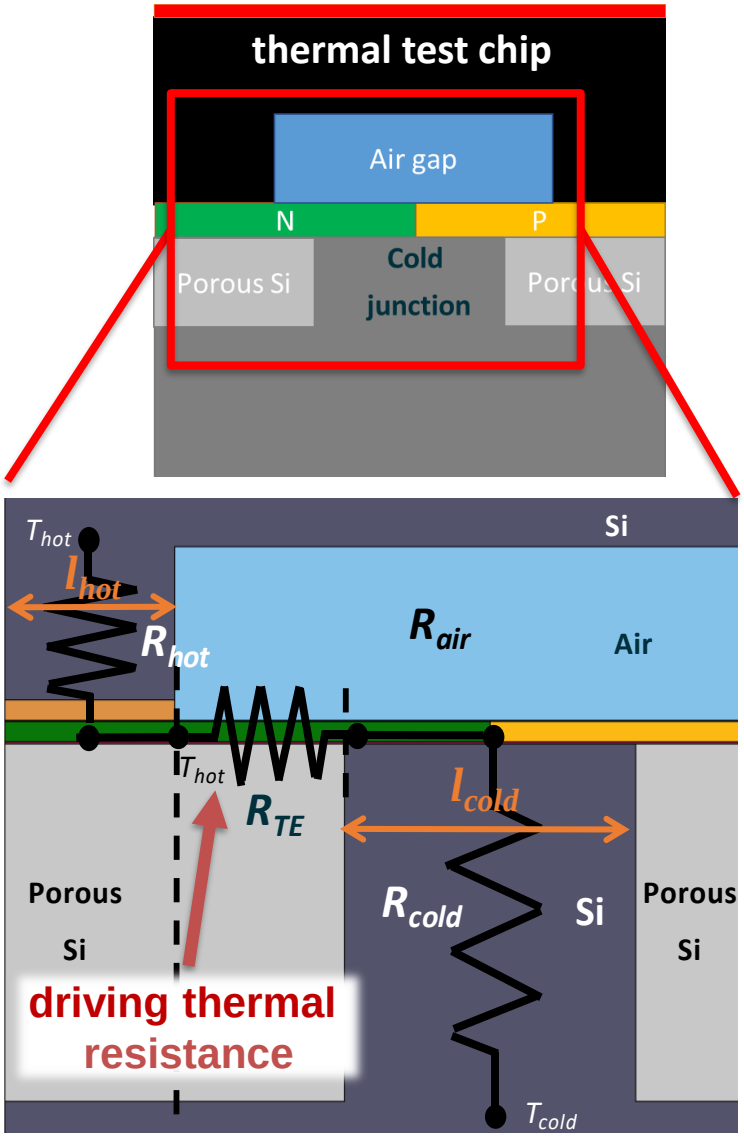
trade-off: harvested energy ($R_{TE,th}$ ↑)

↔ cooling efficiency ($R_{TE,th}$ ↓)

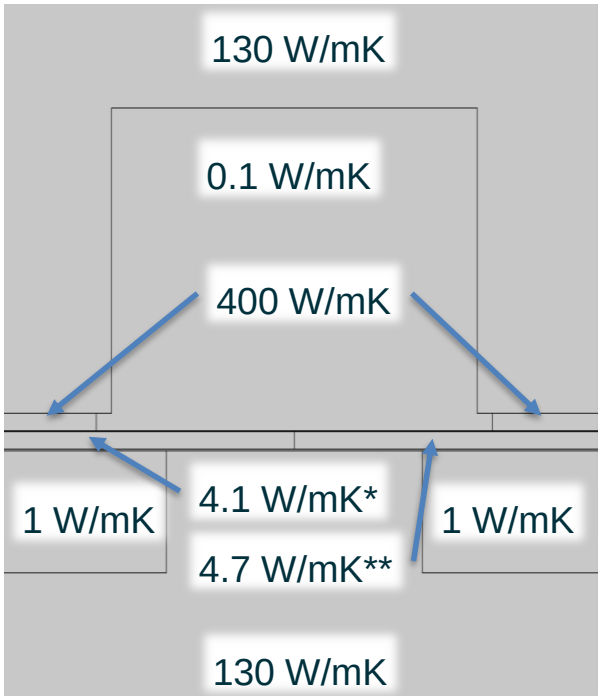
$T_{chip,max}$ = 85°C

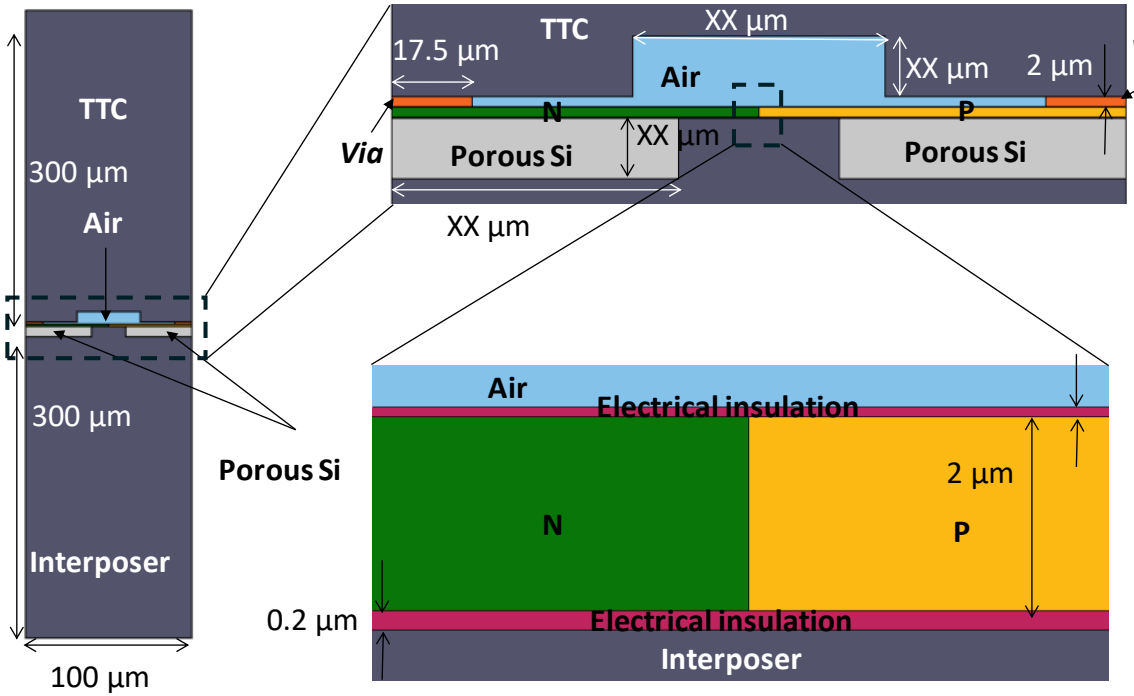
→ Adapt the thermal resistance $R_{TE,th}$ of the thermo-element by adapting the lengths of the air gap and the porous silicon.

Thermal resistance of the thermo-elements can be adapted easily!



Design µTEG – Thermal Conductivity

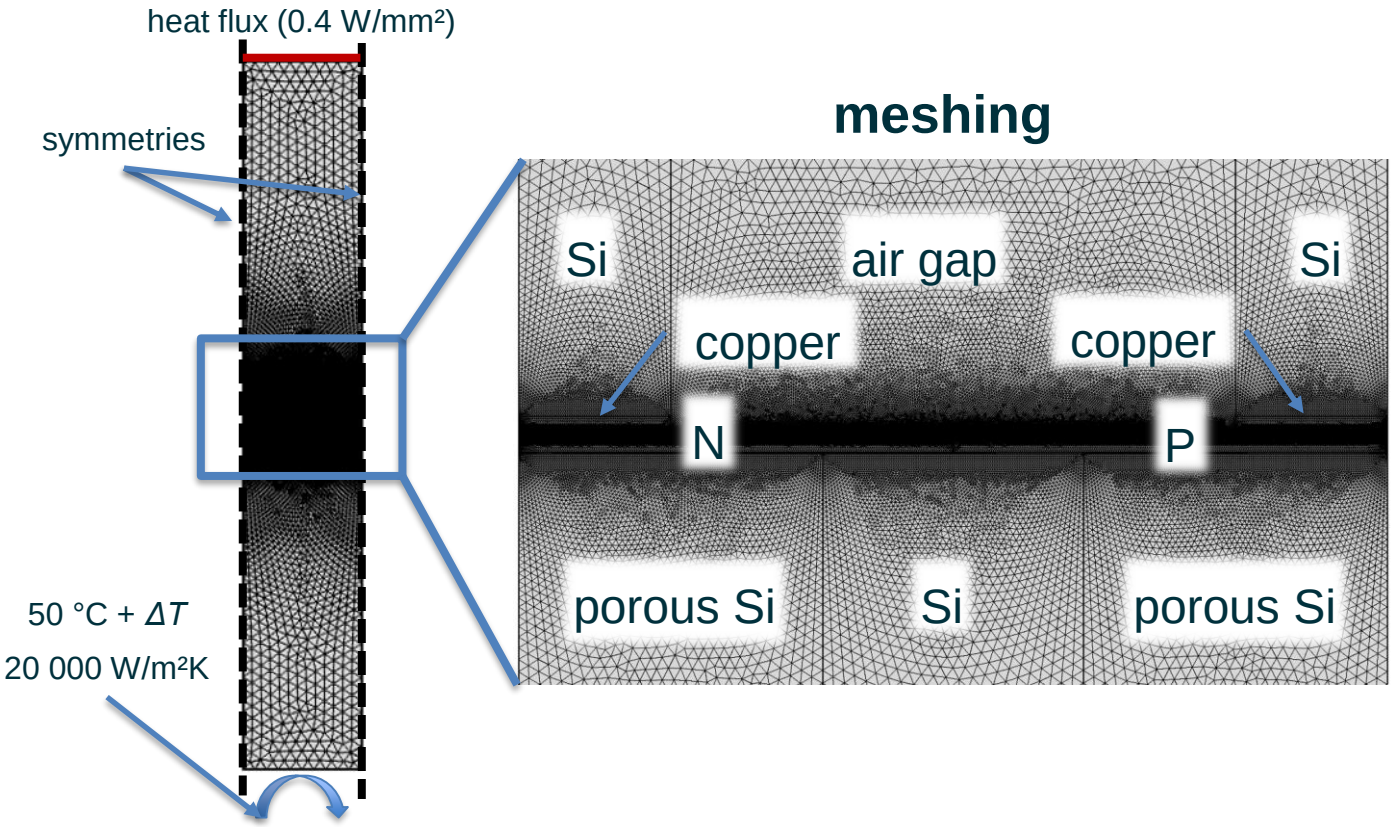




* 5.0 W/mK (QDSL)
** 5.3 W/mK (QDSL)
electrical insulation: 1.4 W/mK

Simulation Model

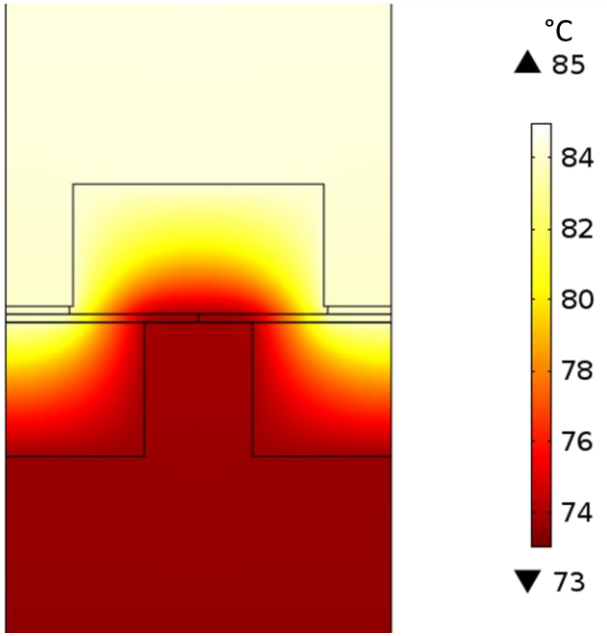
2D module based simulation model (COMSOL) of the thermo-element



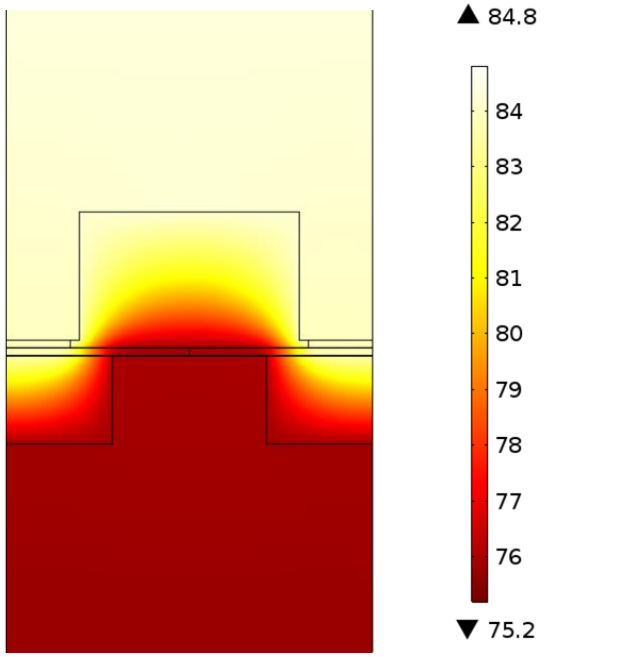
Design µTEG – Simulation Result

QDSL: ΔT = 11.2°C, U_{TE} = 5.24mV **SiGe :** ΔT = 9.8°C , U_{TE} = 5.57mV

cal.: ΔT = 18.0°C, U_{TE} = 9.40mV **cal.:** ΔT = 13.3°C , U_{TE} = 4.47mV



average temperature of cooling fluid: 56.5 °C



average temperature of cooling fluid: 58.7 °C

Using SiGe, harvesting a power of 1mW should be feasible!

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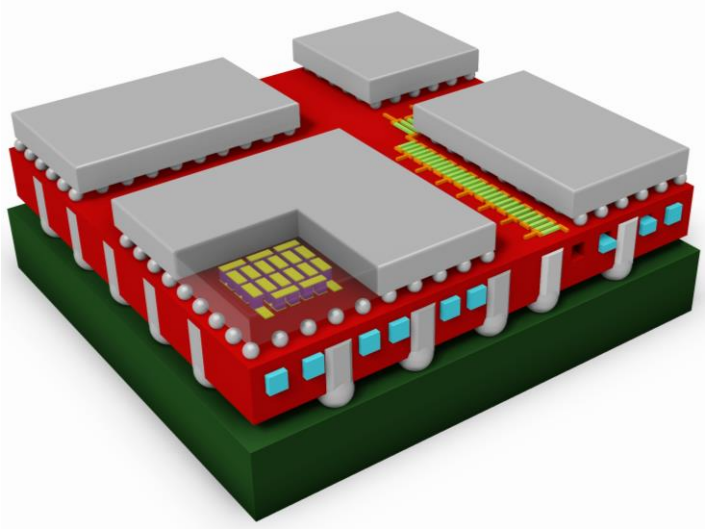
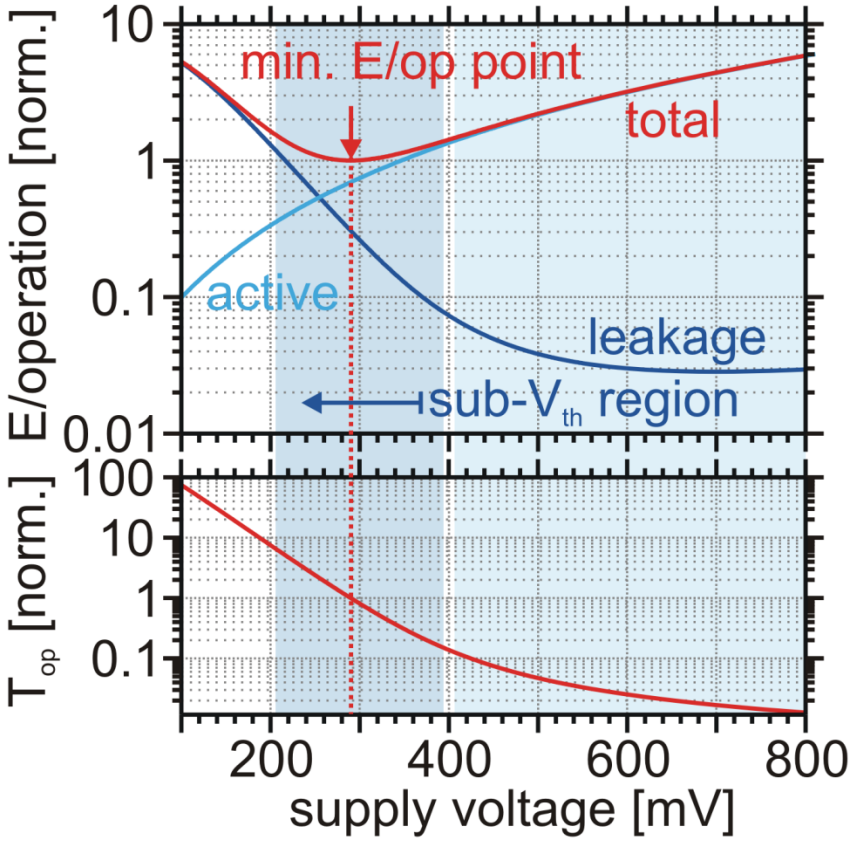


Supply Voltage Scaling – Minimum Energy/Operation

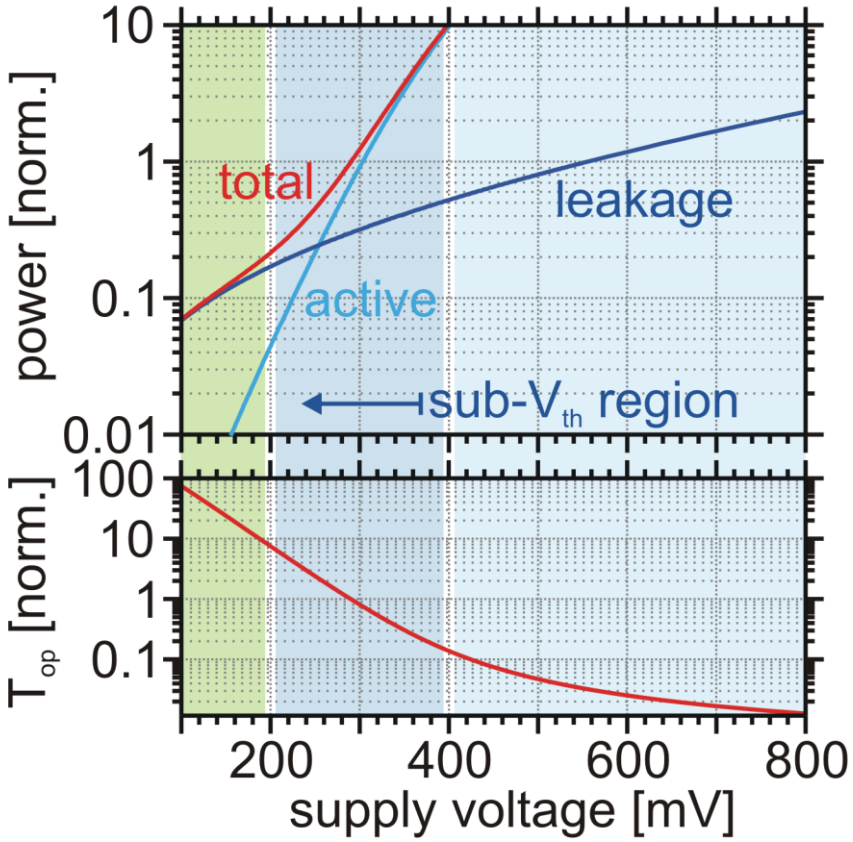
- **low voltage / low power**
  above threshold
  → 500mV < V_{DD} < 1000mV
- **minimum energy/operation**
  near-threshold
  → 200mV < V_{DD} < 400mV



Example: 130nm technology, $V_T \approx 250$mV

Supply Voltage Scaling – Minimum Energy/Operation

- **low voltage / low power**
  above threshold
  → 500mV < V_{DD} < 1000mV
- **minimum energy/operation**
  near-threshold
  → 200mV < V_{DD} < 400mV
- **minimum power**
  sub-threshold
  → V_{DD} as low as possible

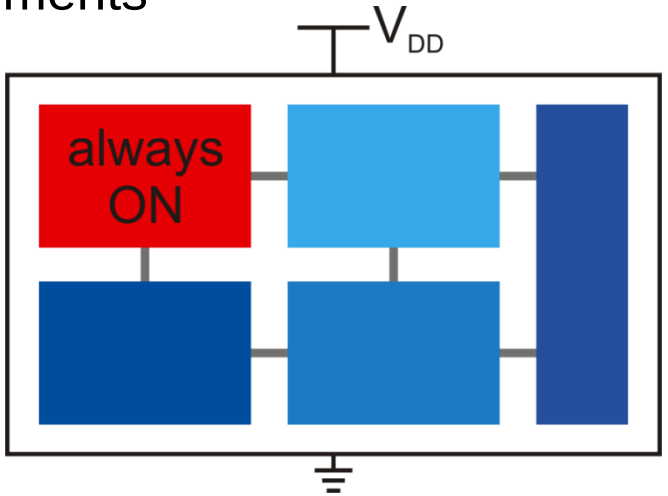


Example: 130nm technology, $V_T \approx 250$mV

Motivation

Why supply voltage reduction below minimum energy per operation point?

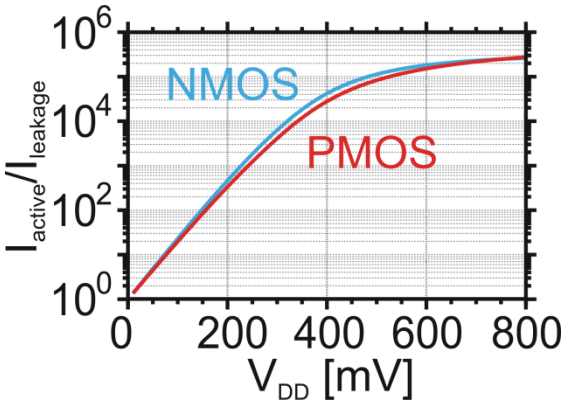
- always-on circuits with low speed requirements
  - wake-up circuits
  - state-holding elements
  - → reduction of stand-by power

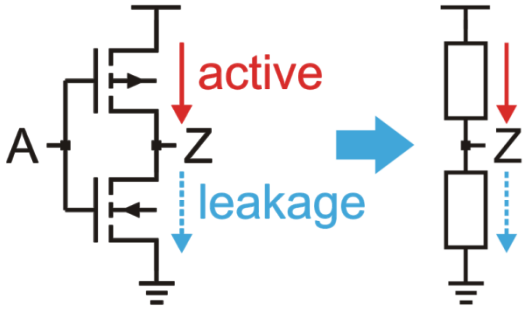


- only low supply voltages available
  - energy harvesting
  - → thermoelectric generators or fuel cells

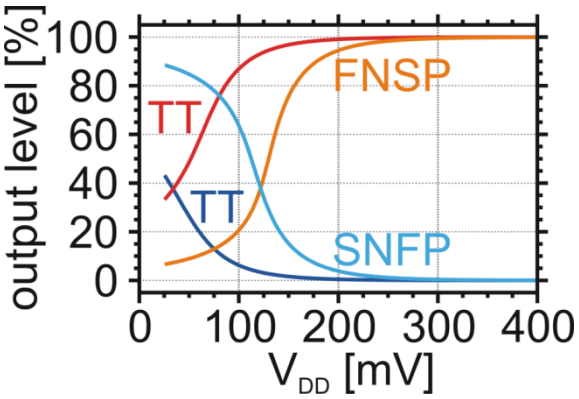
Supply Voltage Reduction – Limiting Factors

- on- to off-current ratio decreases with decreasing V_{DD}





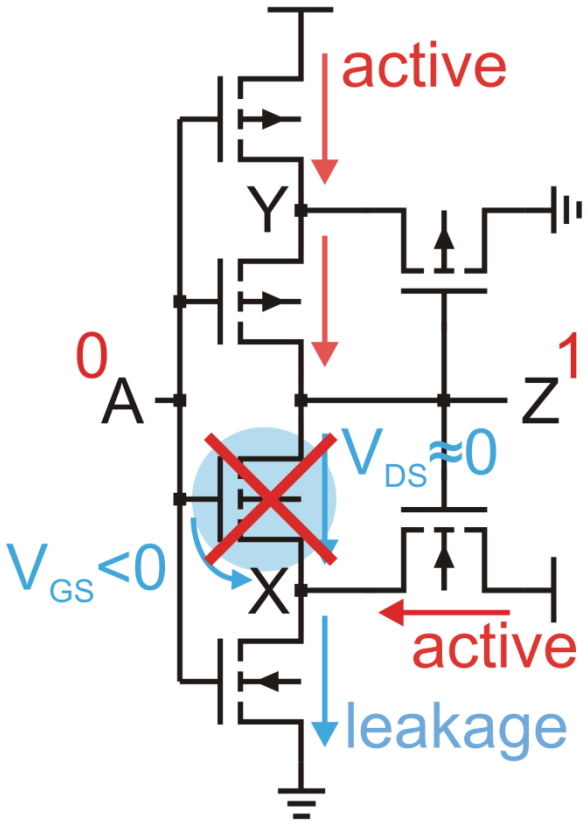
- degradation of output level



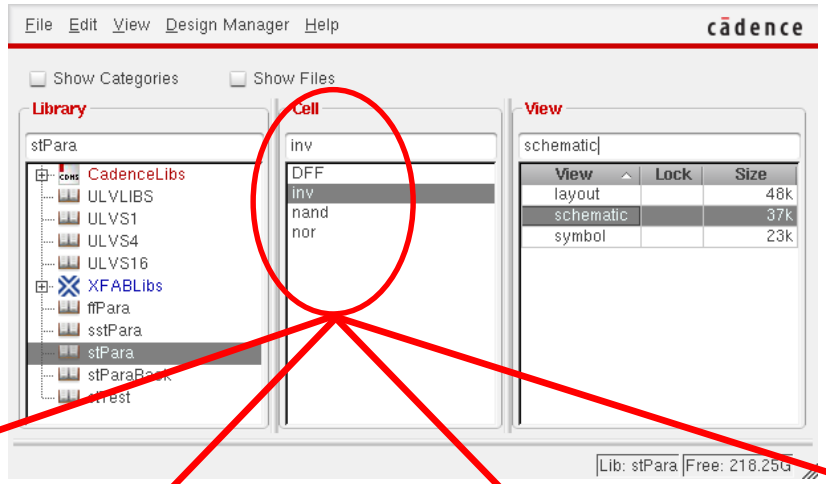
Schmitt-trigger Technology

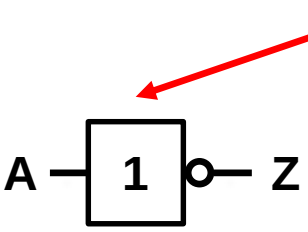
- feedback → node X close to V_{DD}
- V_{DS} of middle transistor close to zero
- V_{GS} of middle transistor below zero

→ leakage quenching

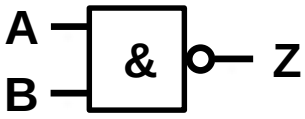


Our Schmitt-trigger Based Digital Standard Cell Library

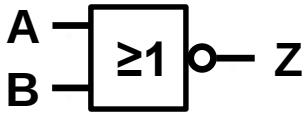




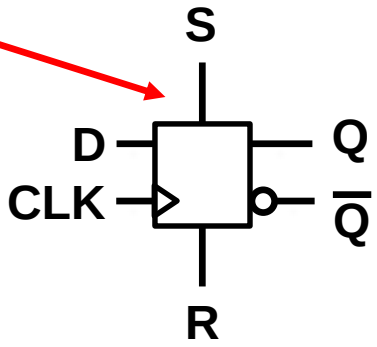
inverter



2-input
NAND



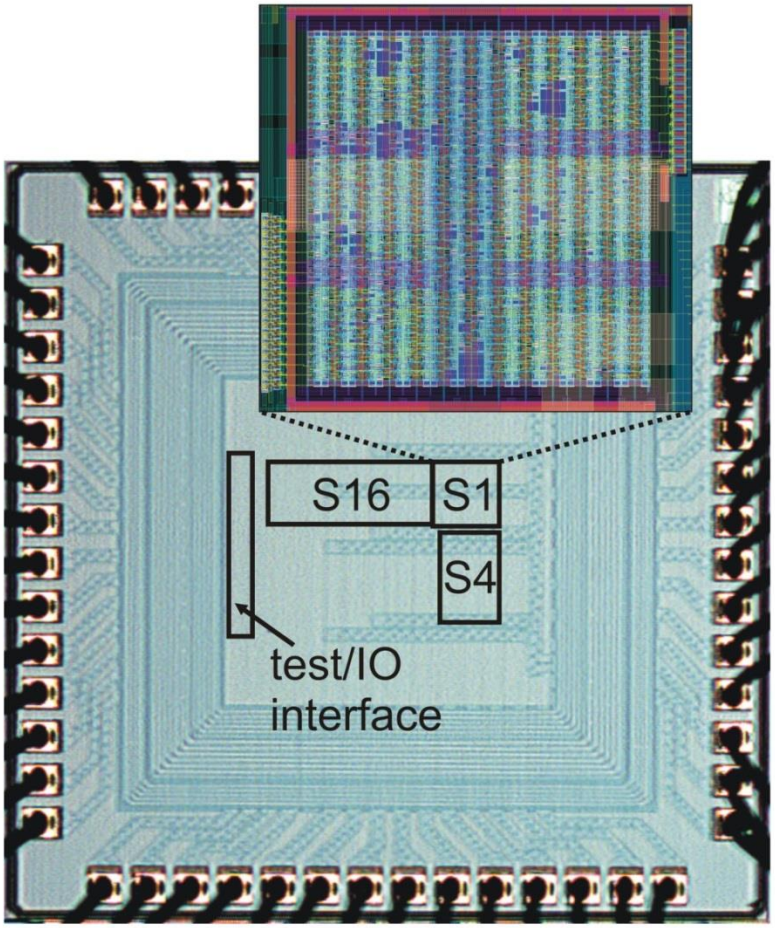
2-input
NOR



D-flipflop
with set / reset

Our Benchmark Circuit – 8b x 8b Multiplier

- silicon area
  - S1: 141µm x 136µm = 19176µm^2
  - S4: 127µm x 189µm = 24003µm^2
  - S16: 343µm x 132µm = 45276µm^2
- fully-automated standard-cell design
- **measured minimum supply voltage: 84mV (S1), 68mV (S4), 62mv (S16)**
- **frequency: a few kHz @ 62mV**

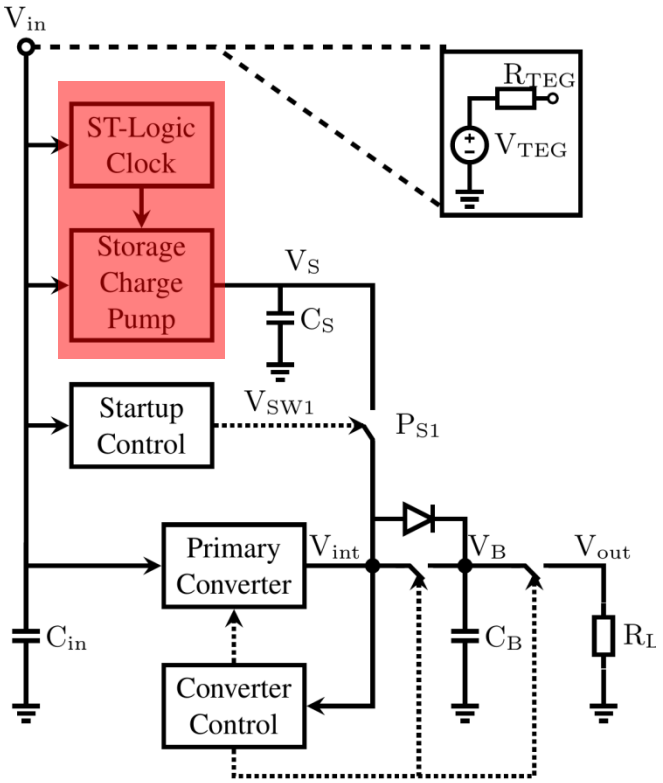


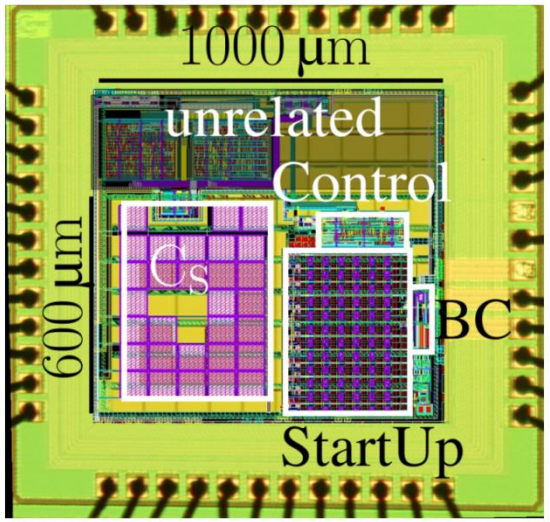
[N. Lotze, ISSCC 2011]

Fully Integrated Startup at 70mV for Thermoelectric Energy Harvesting

low-voltage & low-power charge pump

→ Schmitt-trigger logic based capacitor drivers & control





[J. Goeppert, ESSCIRC 2015]

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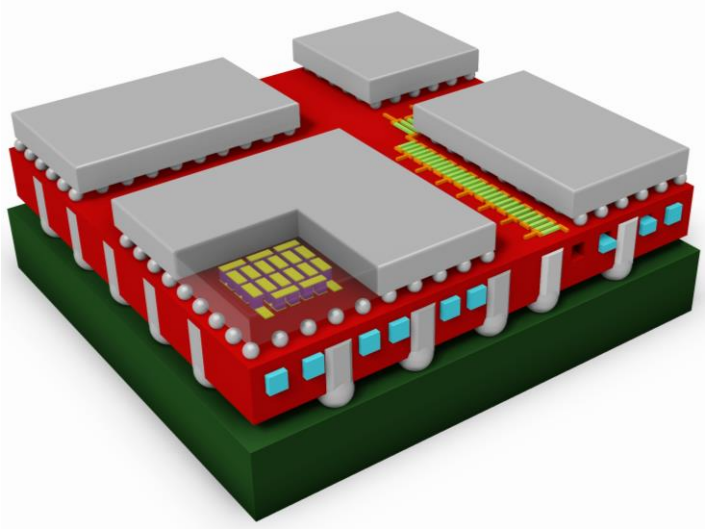

Conclusion

Performing thermal energy harvesting poses challenges on the design & implementation of

- thermoelectric generators
- integrated circuits

Meeting these challenges may pave the way for new integrated energy-autonomous thermal devices!

Thank you for your attention!

The research leading to these results was performed in part within the project STREAMS (www.project-streams.eu) and funded by the European Community's program Horizon 2020 under Grant Agreement 688564.