Integrated Thermoelectric Sensors for Thermal Monitoring of Integrated Circuits

G. Savelli, J.-P. Colonna, P. Faucherand, D. Wendler, Y. Manoli, M. Keller

STREAMS

Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

Therminic2018 – 26-28/09/2018

Contents

- Definition and principle
- Development and results
    - Thermoelectric sensors µTES
    - Read-out interface ROI
    - Joint measurements µTES + ROI
- Conclusions & Perspectives

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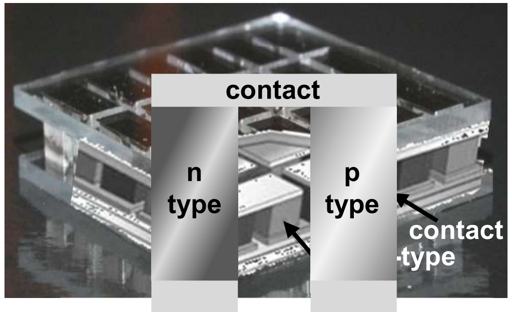
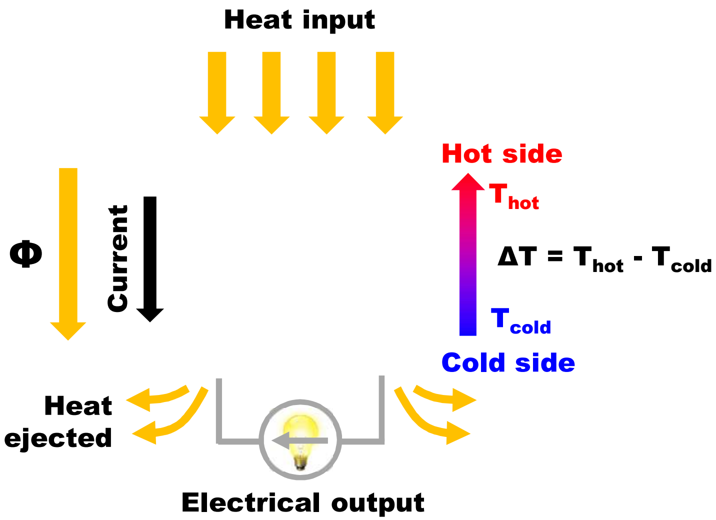
Definition

- **What is a thermoelectric sensor?**

  → Thermoelectric device using Seebeck effect to convert a thermal signal to an electrical signal

Standard structure of TE device in bulk technology.





- **To measure what?**

  → Measurement of thermal flow Φ

  → Measurement of temperature difference ΔT

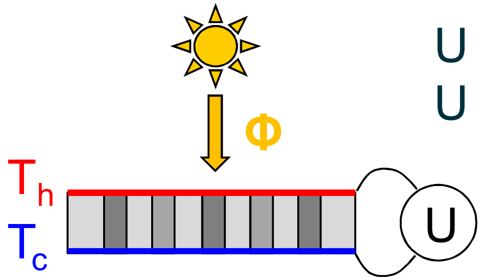
- **For what kind of applications?**

  → Thermal management in microelectronic environment, home automation, automotive, etc.

Principle

- **Working mode of thermoelectric sensor**

→ based on Seebeck effect: power free!



Schematic cross view of TE sensor

$U = N \times S_{np} \times \Delta T$

$U = N \times S_{np} \times R_{th} \times \Phi$

with U = generated voltage (V)

N = junctions number (-)

S_{np} = Seebeck coefficient of one junction (µV/K)

R_{th} = thermal resistance (K/W)

- **µTES: TE sensors in thin film technology**

→ planar sensors (2D)

→ key parameters:

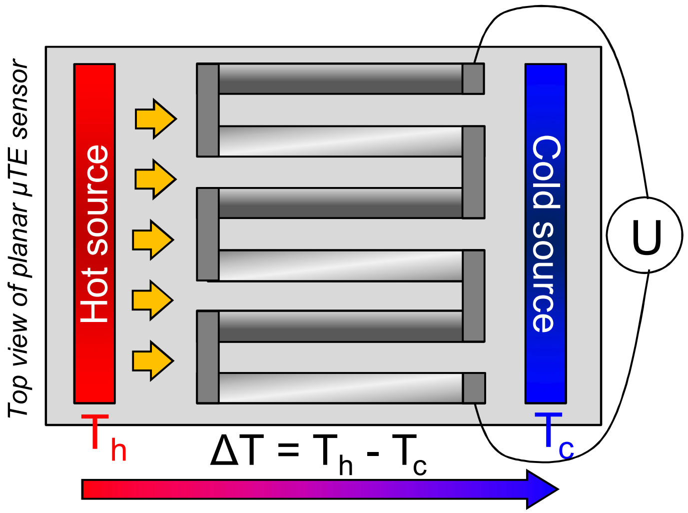
. sensitivity S_e (mV/K)

. area A_{TE} (mm²)

. electrical resistance R_{el} (Ω)

. thermal resistance R_{th} (K/W)

. response time t (s)



→ µTES performance depend on **materials, geometry and environment**

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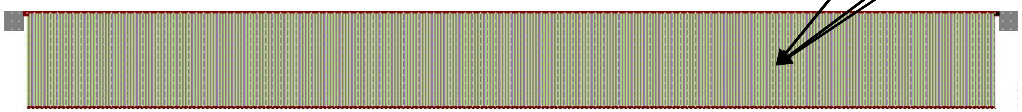
µTES in Project STREAMS

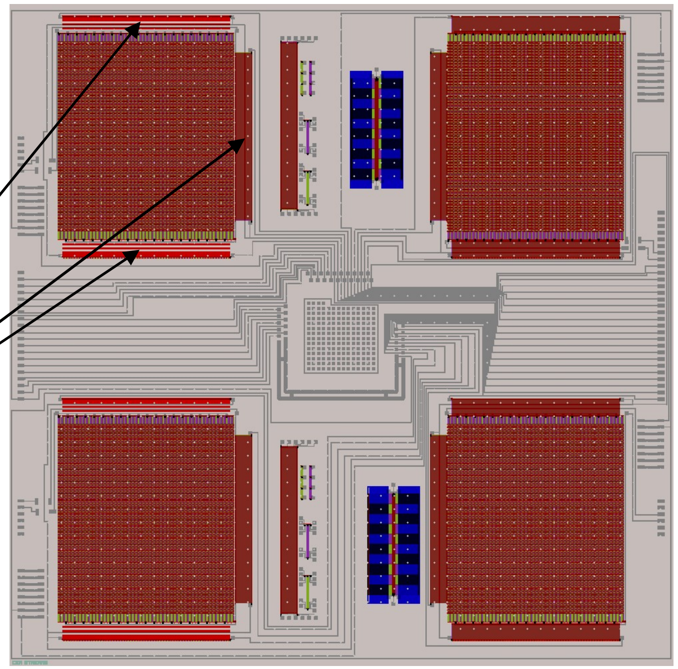
- **Main objective**

  → Integration of IC compatible passive heat flow sensors at the interposer level to anticipate thermal map variation with:
  - a sensitivity Se up to 100 mV/K → *very high signal quality*
  - a response time < 200 ms → *very fast response time*
  - a lateral spatial resolution around 500 µm → *very small area*

- **µTES characteristics and integration**

  → TE materials = poly-SiGe
  → fabrication fully compatible with standard CMOS process flows
  → 12 µTES in total, 3 µTES per TTC
  → all µTES connected to the ASIC





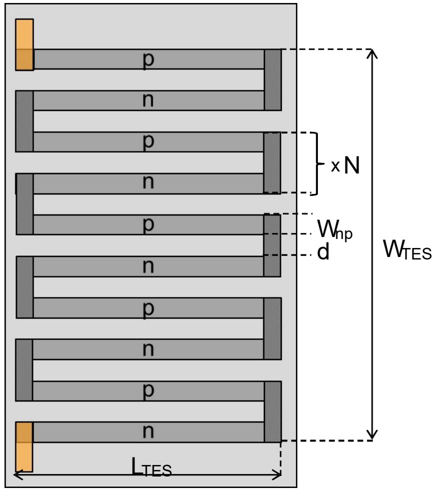
µTES simulation and design

- **Definition of the optimized µTES geometrical parameters**

→ Simulation and design performed using Comsol Multiphysics and dedicated home tool

Main µTES geometrical parameters

Parameters	Values
L_{TES} - Lines length (µm)	**500**
T_{np} – Thickness (µm)	2
W_{TES} - Total width (mm)	5.04



Simulated performances for one µTES at 300K

Parameters	Simulated values
Se (mV/K)	**103**
R_{int} (MΩ)	1.01
t_{Vpeak} (ms)	**1**

→ The 3 mains µTES targets (100 mV/K - 400 ms - 500 µm) should be reached

µTES fabrication

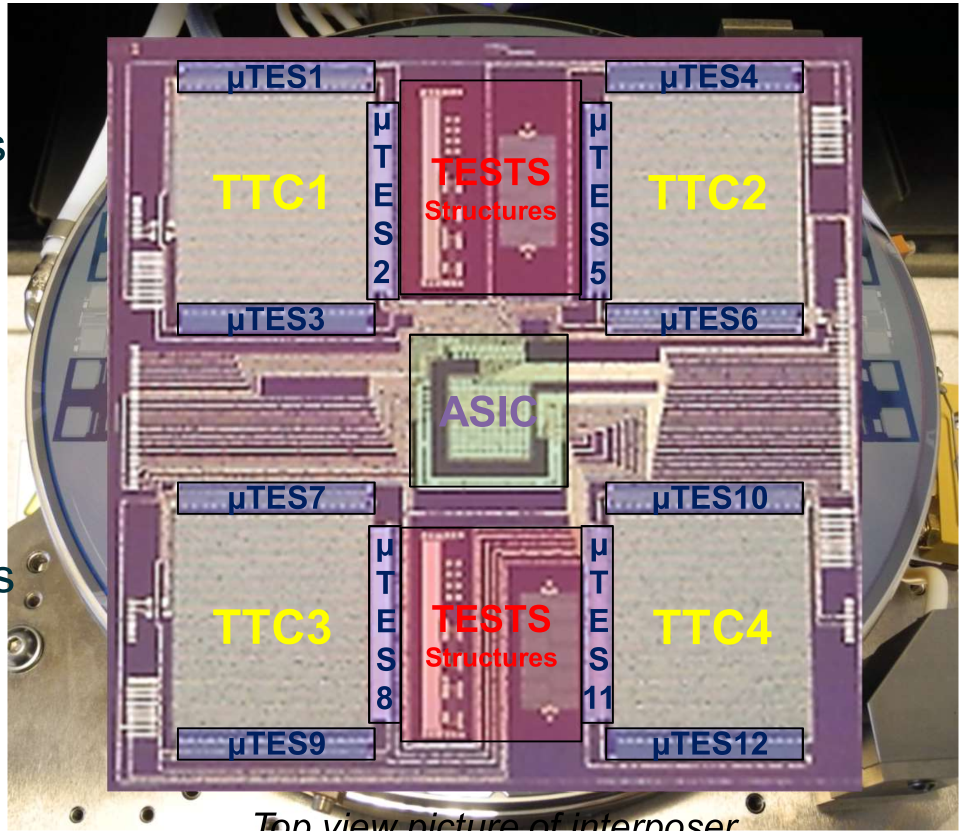
- Technology developed on 8 inches Si substrate
- Silicon-based interposer integrating:

4 Thermal Tests Chips (TTC)
→ designed to allow thermal studies with a strategy of versatile heaters and hotspots in real dice

12 µTES
→ located around each TTC for thermal mapping

1 Application-Specific Integrated Circuit (ASIC)
→ µTES read-out interface for signals management

2 Tests structures areas
→ structures to control TE materials and process flow

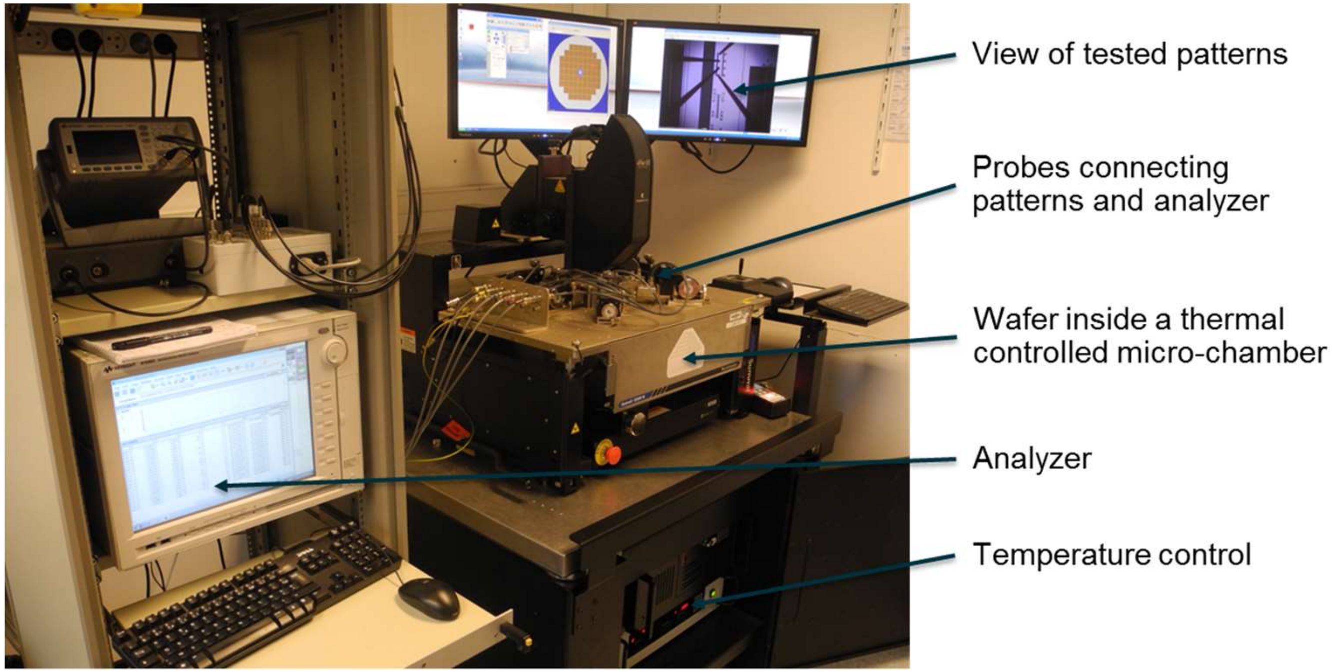


Top view picture of interposer
Picture of a processed wafer

µTES characterization

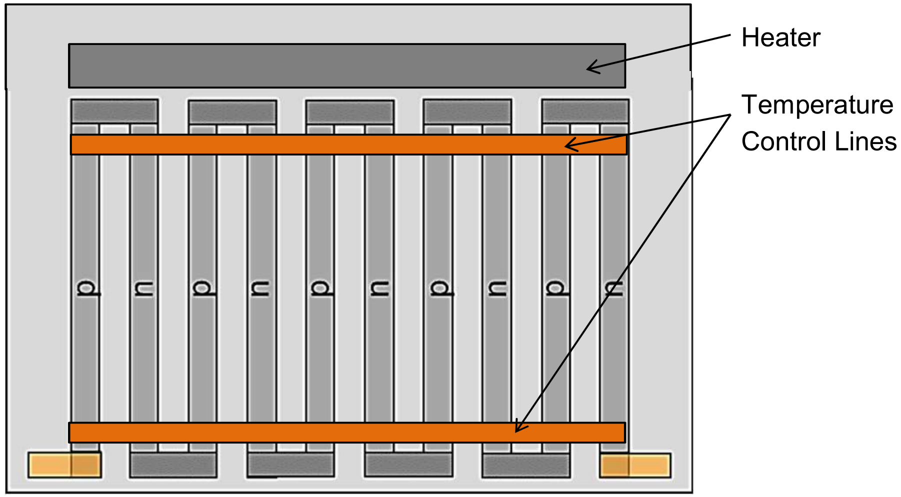
- **µTES characterization**

  → Characterization tool: probe station used for the TE materials and µTES characterization

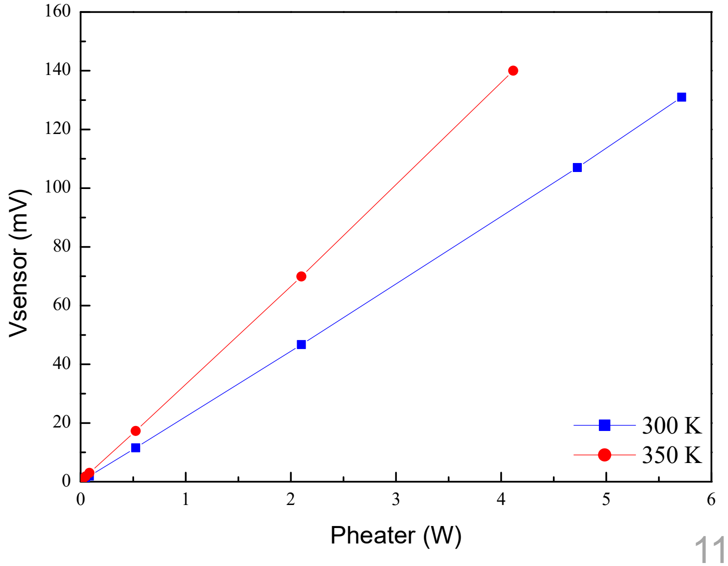


µTES characterization

- **µTES test structures measurement**



Poly-SiGe TTES	Values
R_{TTES_meas} (MΩ)	0.96
R_{TTES_th} (MΩ)	1.01
Se_{TTES_meas} (mV/K)	110
Se_{TTES_th} (mV/K)	103



→ measured values correspond perfectly with expected values

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Read-Out Interface (ROI)

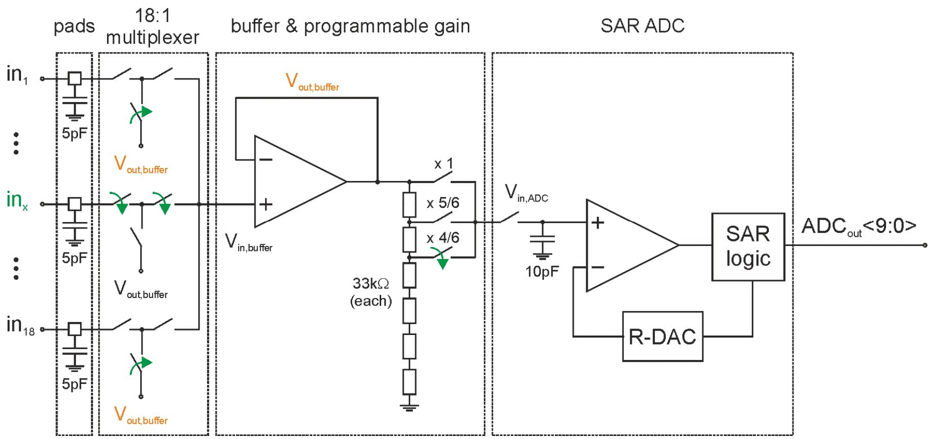
- **Implemented mixed-signal ROI**

→ implemented mixed-signal ROI consists of
  - an 18:1 multiplexer
  - a buffer with programmable gain
  - a 10-bit successive approximation register analog-to-digital converter

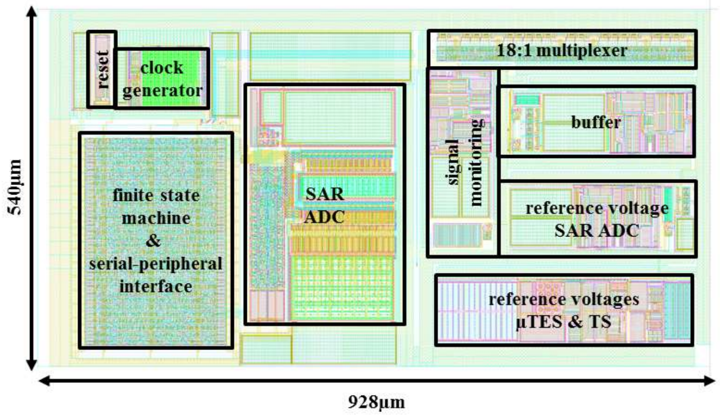
→ read-out and digitization of signals controlled by a finite state machine

→ data transfer from or to the ROI performed by a serial-peripheral interface

Schematics of ROI



Layout of ROI



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µTES + ROI measurement

- **Test configuration**

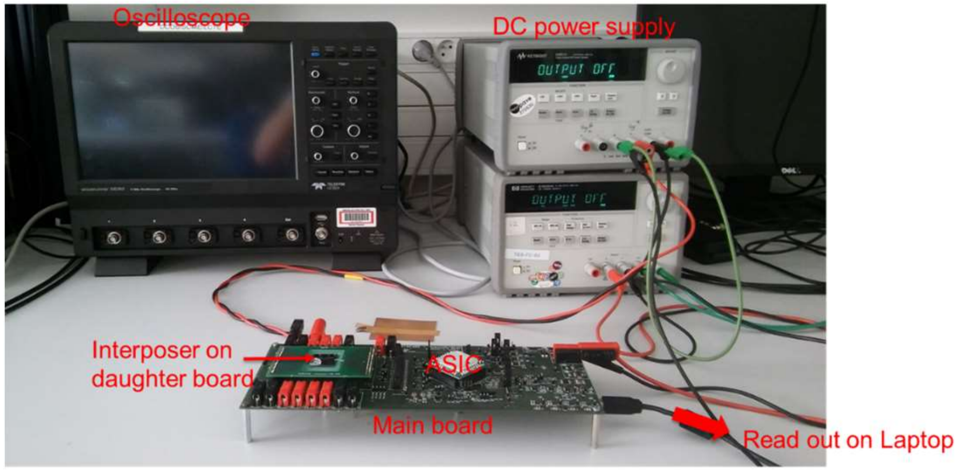
  → Basic scenario:

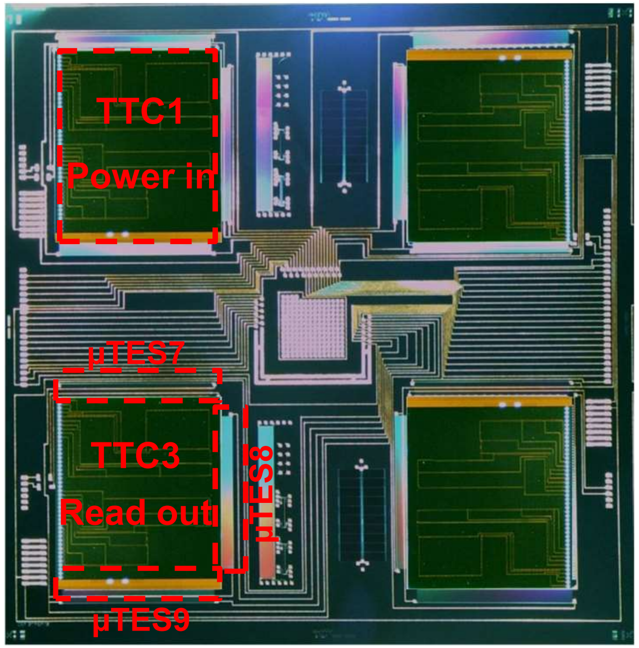
  1 - Power in TTC1 acting as hot source

  2 - Read out the 3 µTES around TTC3 (µTES7-8-9)

  → Steady state & transient measurements

Test bench used for the PoC characterization

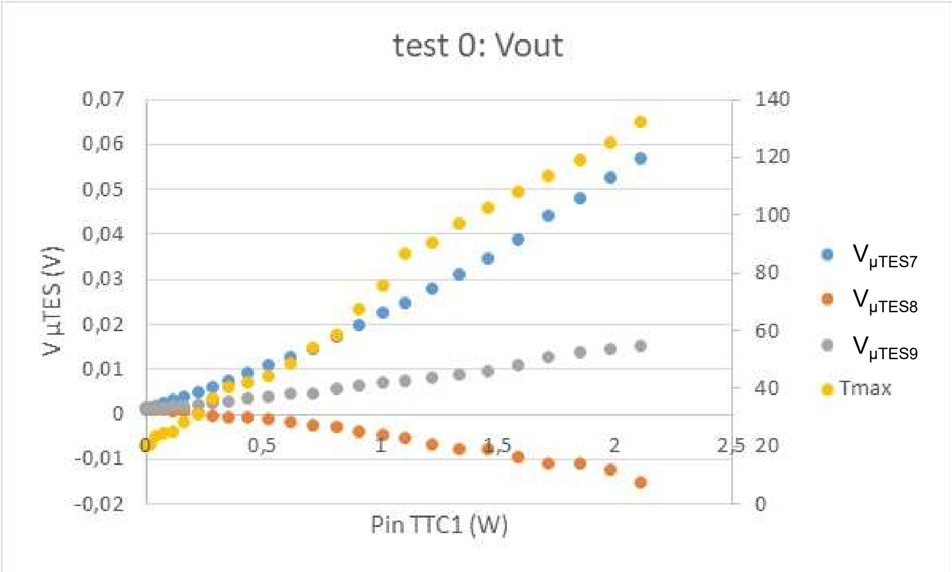




µTES + ROI measurement

- **Steady State measurements**

$V_{\mu TES}$ as a function of power in TTC1

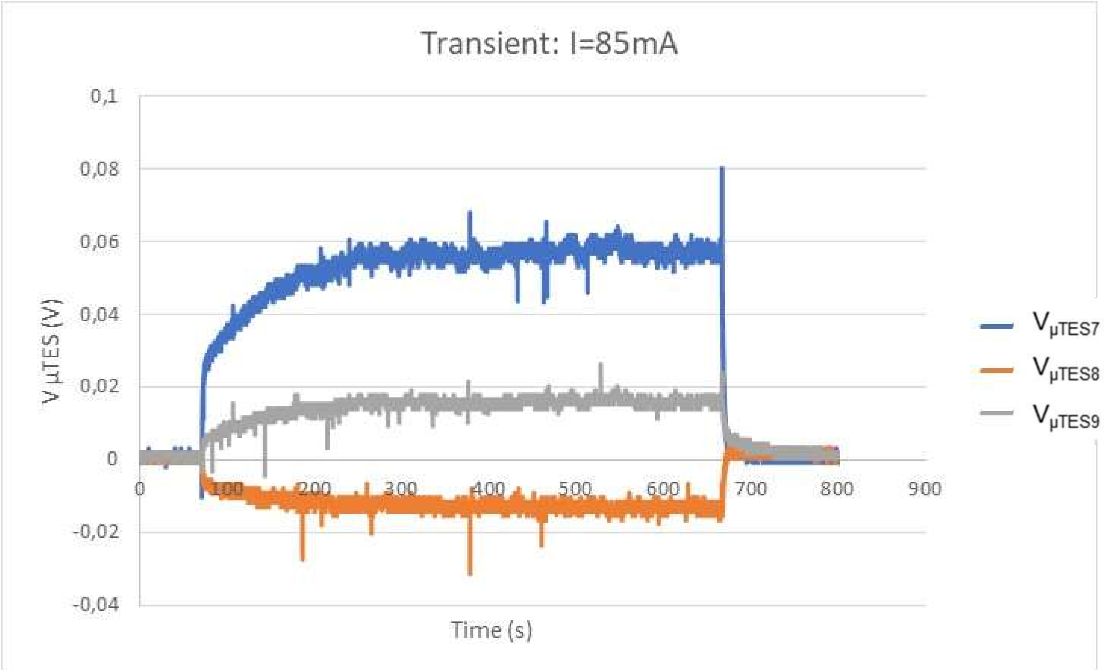


→ $V_{\mu TES7}$ higher than voltage delivered by µTES8 and µTES9 corresponding perfectly with the position of µTES compared to the hot source (TTC1)
→ $V_{\mu TES8}$ delivers negative voltage: orientation of µTES8 (vertical) different than those of µTES7 and µTES9 (horizontal). So the input/output positioning of this sensor is reversed
→ Note: here $V_{\mu TES7}$ = 58 mV corresponds to ΔT = 0.52 K

µTES + ROI measurement

- **Transient measurements**

→ TTC1 heat up then cool down: I_{TTC1} = 0 mA then 85 mA then 0 mA

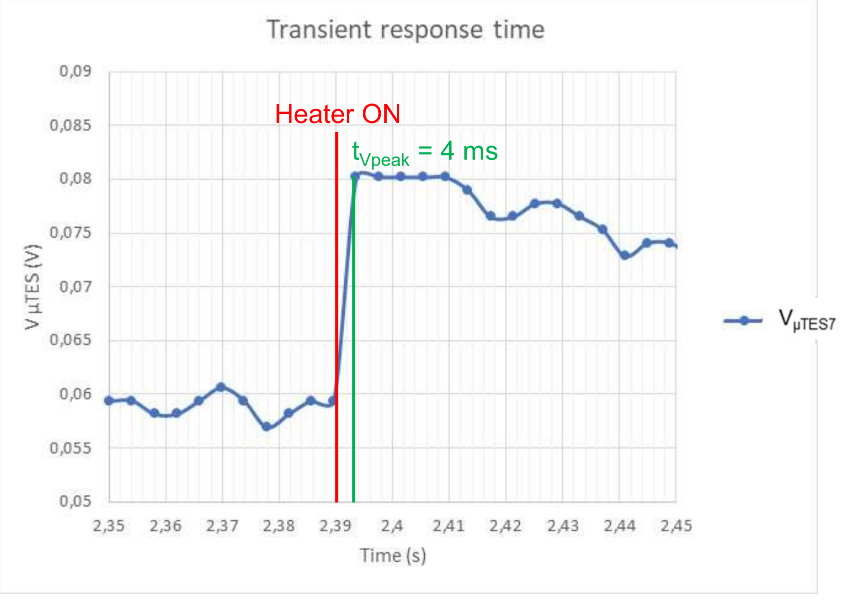


→ same µTES behaviors obtained than in steady state

µTES + ROI measurement

- **Transient measurements**

  → µTES response time



→ Response time ~ 4ms

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Conclusions & perspectives

- **Conclusions**

  → µTES objectives: - a sensitivity Se up to 100 mV/K
  - a time response < 200 ms
  - a lateral spatial resolution around 500 µm

Parameters	µTES STREAMS objectives	Simulated results	Measured results
$L_{\mu TES}$ (µm)	500	500	**500**
Se (mV/K)	100	103	**110**
t_{Vpeak} (ms)	200	1	**4**

→ all objectives achieved!

- **Perspectives**

  → new measurements with more µTES connected to the ASIC
  → new measurements with all TTC working

THANK YOU FOR YOUR ATTENTION