STREAMS

Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

H2020-ICT-2015-688564

STREAMS

Smart Technologies for eneRgy Efficient Active cooling in advanced Microelectronic Systems

Start date of the project: 01/01/2016
Duration: 42 months

D5.3

Performance report of the miniaturized pump-module

WP	5	Generic active cooling thermal management demonstration
Task	5.4	Characterization and reliability tests

Dissemination Level[1]	PU
Nature[2]	R

Due Delivery Date	M36
Actual Delivery Date	21/03/2019

Lead beneficiary	Hahn-Schickard Gesellschaft für angewandte Forschung e.V. (HSG)
Contributing beneficiaries	HSG

Author	Proofreader
Sophie Billat (HSG)	Luc FRECHETTE (LN2)

[1] Dissemination level: **PU** = Public, **PP** = Restricted to other programme participants (including the Commission services), **RE** = Restricted to a group specified by the consortium (including the JU), **CO** = Confidential, only for members of the consortium (including the Commission services).

[2] Nature of the deliverable: **R** = Report, **D** = Demonstrator, **O** = Other.

Document version	Date	Author	Comments[3]
1	18/02/2019	Sophie Billat (HSG)	Creation
2	20/03/2019	Luc Fréchette (LN2)	Modification
3	21/03/2019	Sophie Billat (HSG)	Final version for evaluation

[3] Creation, modification, final version for evaluation, revised version following evaluation, final.

Deliverable abstract

One of the aim of task 5.4 is to adapt the pump module for its integration into the target system taking into account the fluidic interface with the interposer regarding robustness and leakage.
The main subtasks are:

- Verification of the electric communication between the ASIC and the pump discrete electronics in collaboration with UFR-IMTEK.
- Adaptation of the experimental setup for the characterization of the pump with ASICS and the interposer
- Demonstration and test with evaluation of the performance of the miniaturized pump-module with the fluidic resistance of the microfluidic KET.
- Optimization of the PI regulation

The focus of D5.3 is to describe the communication between the black box developed in WP2 and the ASIC like the development and adaptation of algorithms for the pump dynamics considering the fluidic resistance of the microfluidic KET. Afterwards an optimization of the power consumption of the pump-module will be done. More the reliability of the redundancy between flow sensor and temperature management has to be verified and optimized to achieve a standalone temperature control of the entire system.

Table of content

1 – Characterization of the Interposer

Based on the technical achievement of WP2 where we have concentrated our effort in developing pump control parameters and an algorithm based on temperature signal, the ASIC connection and work with the black box electronics like the TTC characterization with KET fluid resistance are developed in the current deliverable.

The interposer

Hahn-Schickard received the interposers at the end of September 2018. The first part of the work was to characterize the interposer itself. An identification of the different resistances is performed by the analysis of photos of the two interposers. We try to follow by the way the wire bonds from the silicon die bond pads and the connections on the interposer itself. Indeed a lot of glue is on the silicon chip as seen on *Figure 1*. For this reason, it was difficult to rapidly define an overview of all the resistances and their connection distribution. Long time was spent to identify these electronic connections. Furthermore, most of the resistances were not able to be measured. The documentation to the electrical connections was difficult to interpret and a few more details were being helpful to finalize the connection matrix.

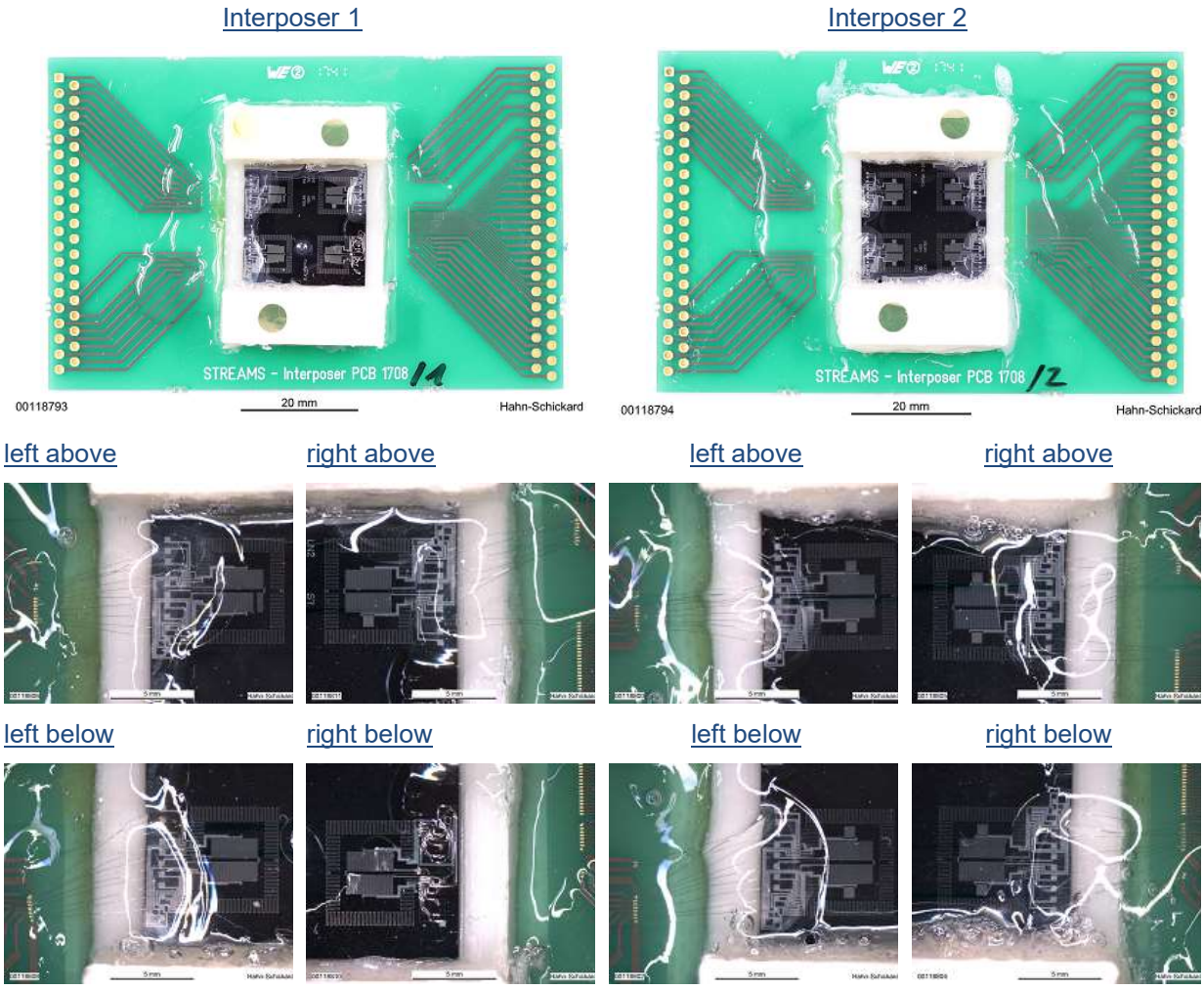

Figure 1: Photography of the delivered interposers

In collaboration with the Université de Sherbrooke, we achieve a clear image of the different elements and their connections to the interposer. During the wire bonding, Sherbrooke faced several challenges regarding the connections, as described in the following:

- Some wire bonds (pin#3) have to cross over others (pin#1 & 2). This creates a risk of short circuit during the epoxy encapsulation. For this reason, we verify the continuity to ensure that there are no short circuits.
- On the "B" device, some of the pads are present on the PCB, but are not electrically connected to the holes on the side of the PCB. In some cases, the bonds to the pads of the chip were done sometime not because of the complexity of the bonding and the amount of them. We try then to verify the connections under microscope to ensure that they are connected to the right places.
- Some devices have simply not been wired due to the fact that the metal layer has peeled of the surface.

We conclude to correct these connections on future generation with the following improvements:
Redesign of the PCB to ensure that all pads are connected to some pins is done like the rerouting of the pin#3 on each device in order to avoid the overlapping of the wire bonds and potential short circuits. On the side of LN2, a change in the process will be adapted to address the peeling of the metal problematic by depositing a dielectric layer over the metal layer.

Electrical data on the connector

In *Figure 2*, the layout of the interposer is presented. The produced circuit-boards we performed in 2018 fits well the one defined by IMTEK. However, the measured resistance values are addressed on other pins than in the mentioned file.

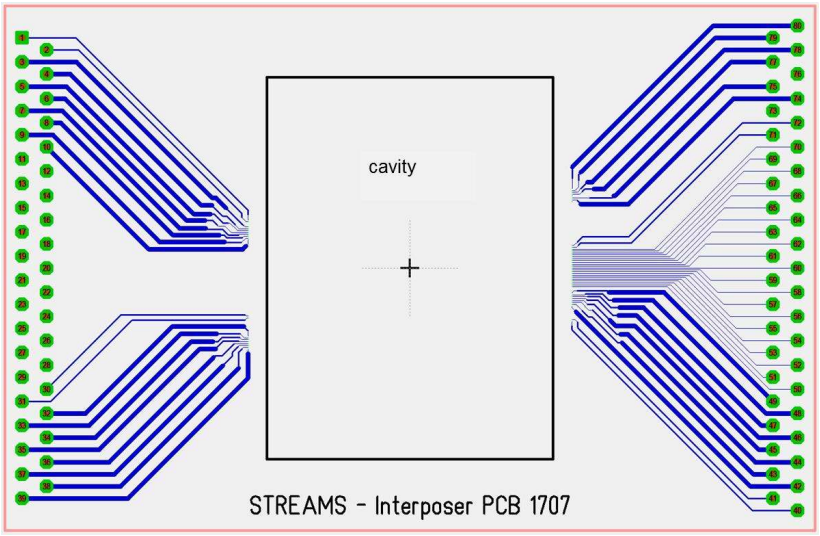

Figure 2: Design of interposer circuit board

At both interposers, the resistance values between all terminals were measured and tabulated. For more clarity, only a small section is presented in the following table:

	Interposer 1										Interposer 2									
	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10
1			29,8																	
2				70,8									77,5	76,7	2,5k	2,5k	1,8k	1,8k	892	892
3														2	2,5k	2,5k	1,8k	1,7k	849	848
4															2,5k	2,5k	1,8k	1,7k	849	848
5						40,1										42,3	2,6k	2,5k	1,6k	1,6k
6																	2,6k	2,5k	1,7k	1,7k
7								124,2										128	953	953
8																			880	880
9										2,8										2,8
10																				

Between pin 7 and 8 an identical value of the resistance for both interposers is found, which could be suitable for temperature measurement. They are underlined in green in the table and connected to input TES 3. These resistors are packed with the entire circuit in plastic bags, immersed in the water bath of the thermostat bath and characterized at two temperatures: 10° C and 50° C.

Calibration coefficients

Previously discrete PT100 sensors were calibrated in order to check the communication between the ASICs and the Blackbox electronics which was developed in WP2. The calibration was done for this aim and the temperature sensors were attached to the assembly board in a cuvette in the thermostatic bath (Julabo F32 HE). The cuvette should be fulfilled with ethanol so that the temperature distribution is really even. The external temperature sensor of the Julabo is inserted into the cuvette too as reference.

In order to calibrate the resistors of the silicon system delivered by LN2 (TTC), the interposer is placed in the same way as for discrete PT100. They are first positioned on the assembly board and both are dipped in the lab's bath in at least three freezer bags for safety. The external PT100 sensor is placed in one of the outer bags (as presented on *Figure **3***).

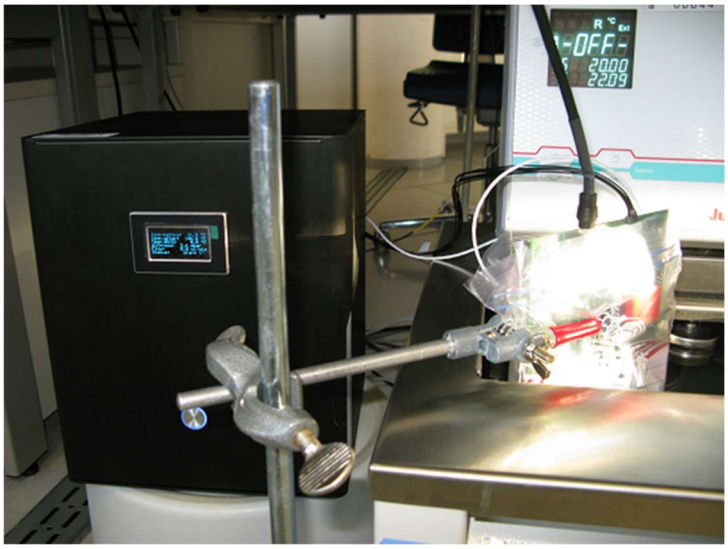

Figure 3: Photography of the experimental setup for the TTC calibration with black box and thermostatic bath.

In order to be able to plug the rather short SPI cable into the black box, it must be located at a suitable height next to the thermostat bath (Julabo). Since the SPI bus is designed for short signal paths between circuits on a printed circuit board, a longer cable cannot be used, communication simply will not work. Actually, the short line used is susceptible to interference, but it is a good compromise for the current alternative.

An adaptation of the calibration program was performed to achieve an automatic calibration of the TTC or PT100 sensors as well as to check a previous calibration. In the first case, the stored coefficients are reset, re-determined and written to memory; in the second case they remain untouched. Before the program starts, Julabo and Blackbox are to be switched on and the communication is tested immediately on initialization. The voltage supply of the assembly board should already be switched on.

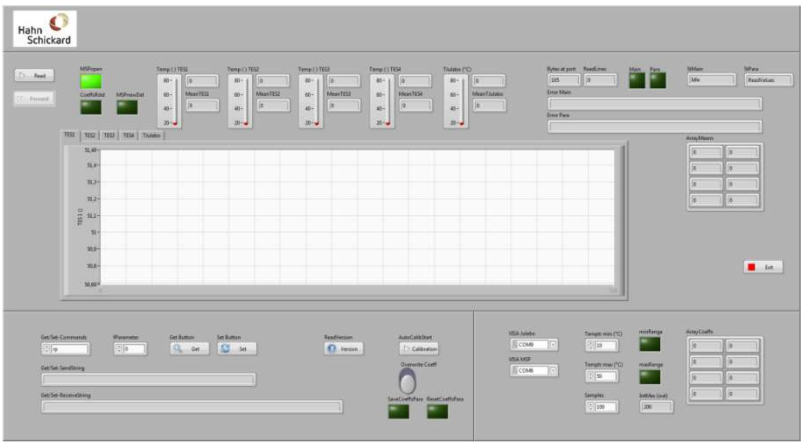

Figure 4: screenshot of the LabVIEW program for temperature sensor calibration

In the following table, the connections between TTC and PCB are summarized with the values of the resistances under the two chosen temperatures of the thermostatic bath. Due to the fact that we were working with metal resistances, we made a linear approximation of the behavior of the temperature resistance coefficient.

Interposer 1 TTC 1 at PCB Stream Assembly 2						
AD-Samples	**10°C**	**50°C**	**Offset AD**	**linear coefficient**	**Connector pin**	**Element**
for TES1	736,76	837,53	-283,452	0,3969	59..73	PT100 DB314
for TES2	696,89	689,72	3898	-5,579	64..73	metal layer 100Ω
for TES3	846,44	943,68	-338,186	0,41135	53..20	Hotspot A?
for TES4	699,33	691,95	3800	-5,42	69..73	metal layer 100Ω

Interposer 2 TTC 1 at PCB Stream Assembly 3						
AD-Samples	**10°C**	**50°C**	**Offset AD**	**linear coefficient**	**Connector pin**	**Element**
TES1	764,7	863,11	-300,79	0,406421	59..73	PT100 IST
TES2	678,98	672,47	4181	-6,144	64..73	metal layer 100Ω
TES3	851,35	939,61	-375,837	0,453206	53..20	Hotspot A? korrigiert
TES4	702,74	696,17	4288	-6,088	69..73	metal layer 100Ω

The green marked coefficients are stored in the µ-controller. Until now it is not so clear why they present so different behaviors considering that they were measured with the same equipment of the analog circuit. With our LabVIEW program the coefficients can be edited. TES2 and TES4 are equipped with fixed resistors 100Ω to test the AD-inputs, but they could also be parameterized. Safe coefficients are chosen as in the next table:

	AOx	**ALx**	**Connector pin**	**Element**
TES2	0	0	64..73	metal layer 100Ω
TES4	0	0	69..73	metal layer 100Ω

2 – Development of the functionality of Blackbox with the IMTEK ASIC

The temperature sensors on the ASIC board are calibrated and the correction data stored in the memory of the black box. The next step is the characterization of the controller at the measuring station. The interposers provide a resistor structure per segment, which has a sufficient temperature coefficient to be able to measure in the chip, and the basic resistor with 125 Ω matches the current

source. Alternatively, a PT100 sensor was attached to the interposer which could provide the feedback to the controller.

The carrier board `Streams Assembly` is designed for four segments of the interposer, each with a temperature measuring resistor. Since some segments are defective, the TES channels can be used for additional PT100. However, the control algorithm in the µ-controller always works with the highest temperature value; here, an unoccupied input could interfere. The open inputs can be shut down simply by clearing the associated calibration coefficients.
The electrical connections of the different devices are presented with simplification in *Figure 5*. The temperature controller runs on the MSP µ-controller in the black box. The µ-controller receives the temperatures in the form of AD digits from the ASIC and calculates them with the calibration data in standard units. Then the highest temperature value is passed to the regulation algorithm. The flow velocity is not sufficient to set the turbine sensor in the black box in rotation, so an additional thermal flow sensor is built into the water loop to performed correct measurement. Our flow sensor needs a long way tube in this measurement range. The experimental setup deals with high flows and by the way in order to minimize or avoid turbulences the income way must be long enough. Due to the fact that this correlated tubing to the sensor presents big dimensions, it cannot be integrated into the box (the delivered long connecting hoses of the flow sensor may not be shortened to not affect its function). Furthermore, the flow sensor was not tested during a long period of time until now and we do not know the life time of the sensor itself in water by such flow rates. For this reason the sensor is not suitable for a durable integration in the blackbox.

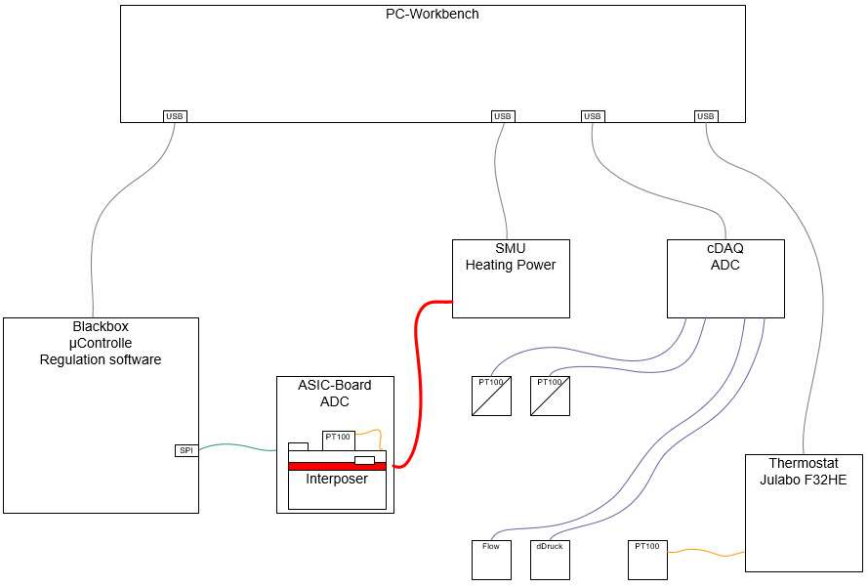

Figure 5: configuration of the electrical connections in the experimental setup with the different part of the systems for characterization

Fluidic circuit diagram

In order to perform correct calibration and measurement with the ASIC, the internal sensor of thermostat is placed outside of its circulating pump. It is disassembled to calibrate the interposer temperature sensors and placed with them in the bath. It must always be in contact with the cooling medium; otherwise the control circuit of the thermostat is open, which means that it cools down with maximum power. The configuration of the fluidic circuit diagram is schematic presented on *Figure **6***.
For the measurements the flow sensor was placed up streams between heat exchanger and the interposer.

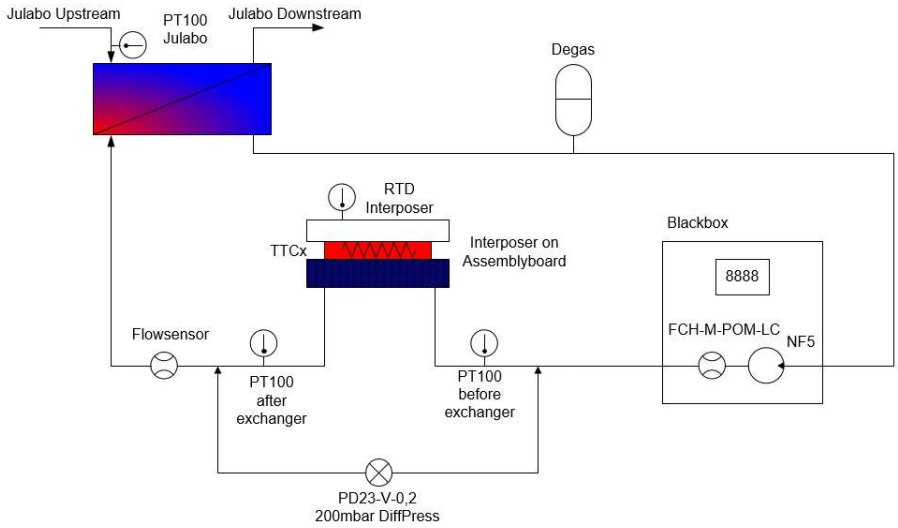

Figure 6: Fluidic portion of the experimental setup with the different part of the systems for characterization

Labview measurement setup software

The aim is to demonstrate the energy-saving potential of the µfluidic structures of our project partners. The MEMS "setup" should consist of several silicon layers: a thermal test chip simulating the heat output of a processor, µfluidic channels with fins and valves for flow control, and a TES layer for local relative temperature measurement, RTDs for absolute temperature measurement, and thermoelectric generators (TEG) for energy recovery. According to the current project status, a configuration of black box, assembly board with ASIC and a TTC is required. The temperature sensors are calibrated and the coefficients are stored in the µ-controller. An optimization for the regulation of the cooling system has to be found, taking into account the different reaction times of the different components of the fluidic circuit.

The communication between PC and peripherals requires different cycle times: the thermostat can supply a maximum temperature every 250ms upon request, the blackbox sends data asynchronously, the buffer must not overflow, which requires a complicated time management for the communication to the µ-controller. To avoid this problem, the temperature of the Julabo is cyclically interrogated after program start until the specification is reached, then a PT100 sensor is used on the NI cDAQ module and communication with the Julabo is terminated. The connection between the PC and the black box is checked with the hyperterminal to control the functionality of the communication and ensure data transfer. A display of communication is added to the Labview program simply by placing the buffer level on an indicator. The program deals with the different deadtime and different reactions time of the circuit elements.

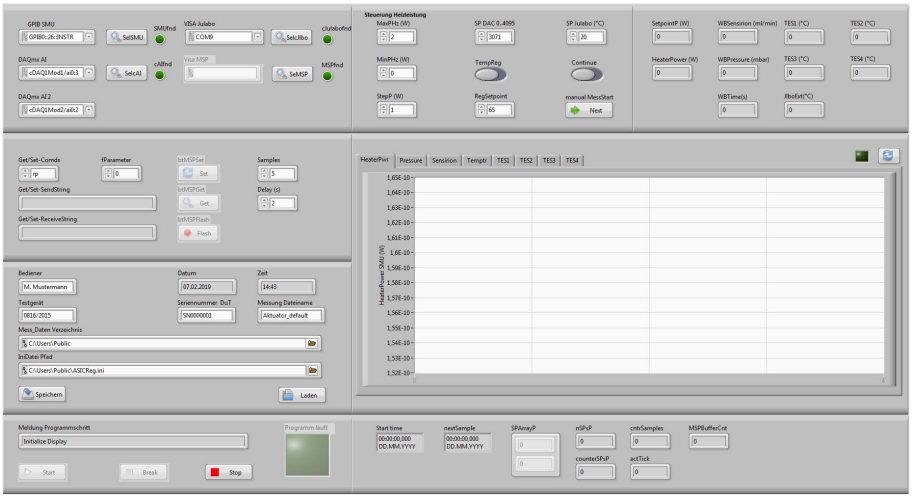

Figure 7: screen shot of the Labview program

Measurement of the STREAMS Interposer 1

First, it is carefully determined which heating power is allowed to be applied on the resistances. In addition, for the dimensioning of the used heater structure, the heating power has to take into account the pumping speed and in particular the bubble-free filling of the complete water cycle. This is important to avoid an unintentional local high temperature increase, which can destroy the structure. One can specify the maximum pump speed (TempReg = off) and thus determine which maximum heat output can be dissipated until the highest temperature at TES1.4 has risen to 70 °C. The 70 °C limit is an empirical value to control the experiment without damage.

For the first measurements on Interposer 1 from TTC1 or TTC A, a resistor is used as temperature sensor and another one as heater. The selection was made according to resistance values, sensor approx. 120 Ω cold at pin 7-8, heater approx. 40 Ω at pin 5-6. These resistances are not the ones which were assigned for the aim according to the initial bond plan. The resistances correspond to the hotspot and Heater Central respectively. The temperature sensor was then calibrated as described

After applying a heating power of 5W, the temperature measuring resistor did not produce a signal and its resistance value increased over 200 kΩ. This behavior is not really traceable because if an overheating occurs, only the heating resistor should be affected and not the measuring resistor one. Visually, no damage was seen. In order to find the source of this behavior an optical inspection was performed. No damage could be identified. To avoid this problem TTC 3 resp. TTC C temperature were calibrated. The selection of the structures was made according to resistance values, with a sensor approx. 104 Ω cold at pin 36-37 and the heater approx. 39 Ω at pin 34-35.

Since we only have one interposer with two usable TTCs we decide to work with a relatively low heat output (max 3W). To characterize the TTC structure, the heating power is varied and the temperature is recorded at TES 3 at constant pump speed. During the first measurement it was seen that the resistance signal was not stable and by this way it is difficult to have a good regulation. In order to obtain stable results and optimized the pump modulation algorithms we try to glued a 39Ω SMD resistance on the TTC itself to perform reliable measurements. Unfortunately, the thick epoxy layer seen for the mounting of the interposer (*Figure 1*) covered also the TTC resistor structure inducing an extremely poor thermal coupling. For the reason the way used with the glued SMD resistance is not optimal for the characterization of the black box controller on the TTC.

The measurements are not consistent until now. But it is to underline that the fabrication of the interposer is complex and represents a big challenge. With this first run, we achieved nevertheless exploitable results concerning the regulation algorithms as presented in the next paragraph. The final optimization to reduce the hydraulic power will be done with the new interposer generation in close cooperation with UdL (Lleida).

Characterization of the Blackbox controller with Interposer 1

Due to the different problems discussed before we are still trying to achieve measurement to define the efficiency of the Blackbox controller. An SMD resistor and a PT100 sensor are glued to position TTC2 to have the possibility to test the control loop with the small dimensions of the fluidic chip.
Already 1W heating power is enough to raise the chip temperature to 60 °C (***Figure 8***). The higher the allowable temperature, the more efficient the cooling is.

By temperatures higher than 30°C the pump modulation achieves to obtain a constant temperature without need of high power consumption. With an increase of the heating power of the interposer it can be seen that the temperature is successfully controlled and all curves over 30°C present a constant behavior. On the opposite at low temperature, the cooling effect is not efficient enough and the temperature rises (as seen on the violet curve). For a correct cooling a higher pumping power must be needed which is contrary to the aim of the project.

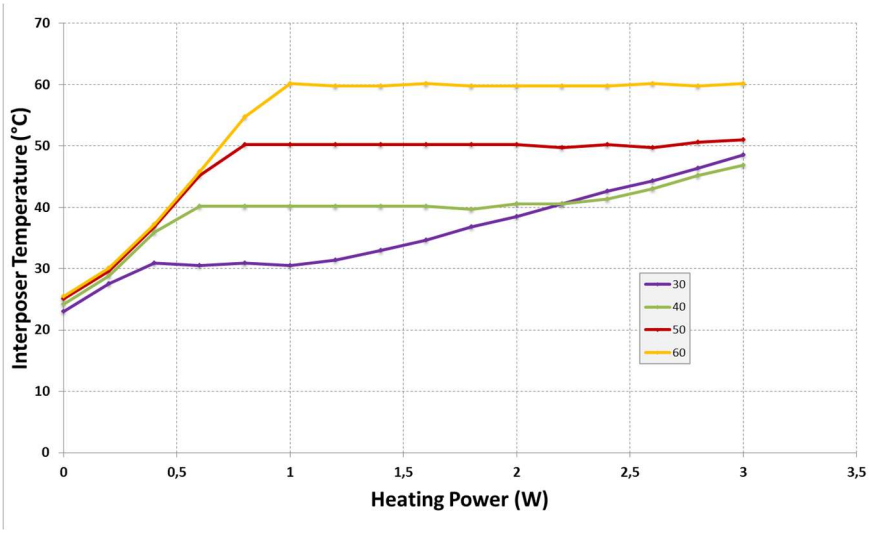

Figure 8: Temperature regulation over heating power. The temperature is given by the ASIC

As presented on *Figure 9* the pump achieves a maximum hydraulic power of 350µW at the TTC (ThermalTestChip).

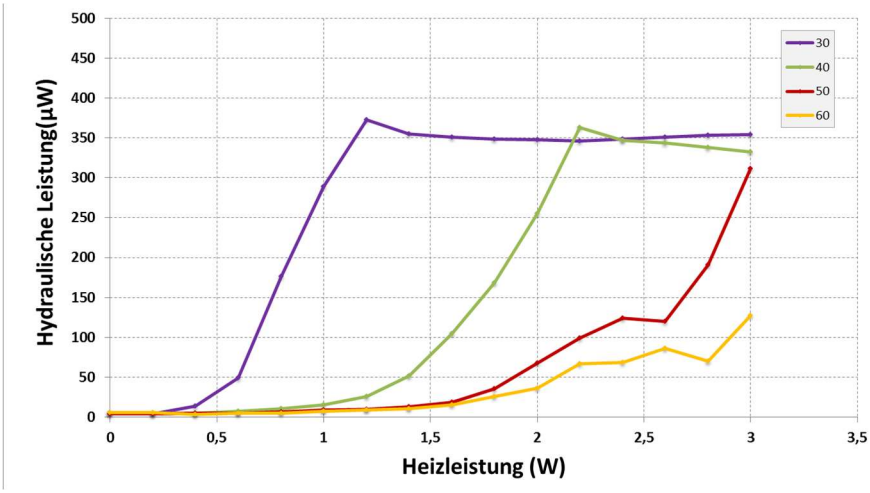

Figure 9: Characterization of the hydraulic power depending on the set work temperature for different heating powers

Thus, a heating power of 3 W can be dissipated, if 50 °C chip temperature is allowed. If the chip temperature can rise to 60 °C, significantly higher heating capacities are possible, in our test setup we are limited by the load capacity of the heating resistors. With only one TTC, we achieved a good hydraulic power showing the good efficiency and the well adapted algorithms of our controller even with the small dimensions of the chip. In the next generation on the interposer with the realized TTCs as planned, the performance through parallel connection is been expected much higher.

Concerning the pump control reaction against the change of the heating power of the interposer to that achieve the constant temperature behavior the results will be done with the final interposer design and will be reported in D5.5.