STREAMS

Smart Technologies for eneRgy Efficient Active cooling in Advanced Microelectronic Systems

H2020-ICT-2015-688564

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Smart Technologies for eneRgy Efficient Active cooling in advanced Microelectronic Systems

Start date of the project: 01/01/2016
Duration: 42 months

D5.5

Report active cooling demonstrator characterization: thermal and energy performances and reliability

WP	5	Generic active cooling thermal management demonstration
Task	5.4	Characterization and reliability tests

Dissemination Level[1]	PU
Nature[2]	R

Due Delivery Date	M42
Actual Delivery Date	18/07/2019

Lead beneficiary	UdL
Contributing beneficiaries	LN2, UdL, CEA, HSG, UFR-IMTEK, ST

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[1] Dissemination level: **PU** = Public, **PP** = Restricted to other programme participants (including the Commission services), **RE** = Restricted to a group specified by the consortium (including the JU), **CO** = Confidential, only for members of the consortium (including the Commission services).

[2] Nature of the deliverable: **R** = Report, **D** = Demonstrator, **O** = Other.

Document version	Date	Author	Comments[3]
v1	17/07/2019	J. Barrau (UdL)	Creation
v2	18/07/2019	G. Savelli (CEA)	Modification
v3	19/07/2019	J. Barrau (UdL)	Final version for evaluation

[3] Creation, modification, final version for evaluation, revised version following evaluation, final.

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1 – Introduction

1.1 – Integration of functionalities

As already explained in previous reports, there is a compromise between cooling and energy harvesting, as the harvesting option includes thermal insulation trenches under the hot thermoelectric junctions in order to maximize the harvested power. But these trenches also increase the thermal resistance between the hot thermal test chips (TTC) and the µ-fluidic back-side. So for the final demonstrator, we have decided to focus on the active cooling functionality and we have chosen to assemble an interposer without the insulation trenches. So the thermo-electric generators, although present on the sample, will not be tested because the harvested power would be very limited.
Our objective with this final demonstrator will be to highlight the active cooling functionalities (WP2), e.g the self-adaptive µ-valves and fins, with the thermoelectric sensors (µTES) embedded in the interposer (WP3).

1.2 – Overall assembly for testing

Detailed reports on the design and manufactured thermoelectric sensor (µTES) are provided in the deliverables D3.2 - D3.4. Detailed process flow for the fluidic layers is presented in WP2. To complete the overall demonstrator assembly, additional processes were required, mostly to bond the TE layer to the microchannel stack. The complete stack is shown in Figure 1. The three layers stacking involves the cell cavities (layer 1), self-adaptive and controlled microfluidic fins and valves (layer 2), and the fluidic inlet/outlets (layer 3). Layer 1 and 2, both in Si, are bonded together using a eutectic Au/Si bonding, while the adhesive bonding using photoresist PERMINEX 1000 has been proposed to bond layer 2 with layer 3 made of polyimide Kapton, contains the fluidic I/O of each cell.
Although the thermoelectrics and adaptive cooling were integrated, only the µTES were tested with the adaptive cooling. The µTEGs require insulation trenches to be efficient, which were not integrated with the microfluidic cooling since they add a high thermal resistance, which is not desirable in conjunction with active cooling.

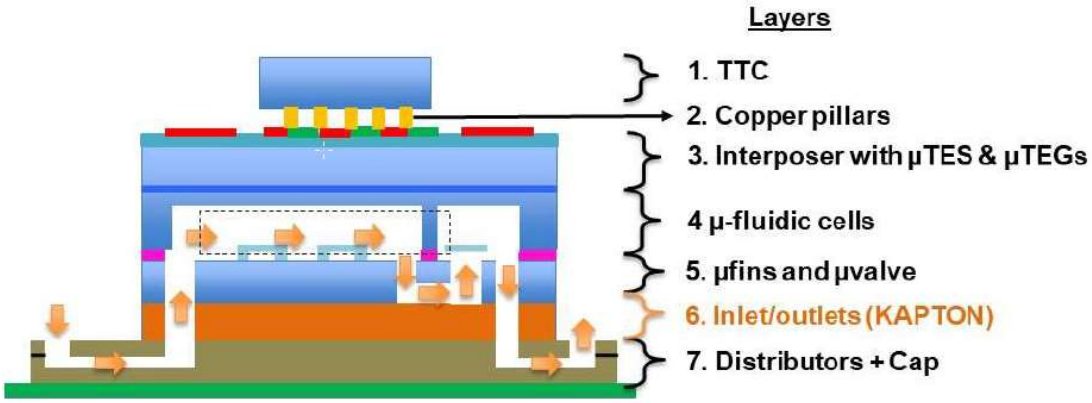


Figure 1 – Schematic drawing of the final assembly.

The device under test have fluid inlets and outlets distributed over the back side. To ensure a reliable supply and collection of water, the chip was packaged over a plastic distribution manifold. Supply and collection channels have different widths only to ensure proper mechanical support of the Kapton under the fluidic layer. The manifold is 3D printed out of ABS plastic using the fused deposition modeling process. The manifolds are then sealed by a quick exposure to liquid acetone followed by a drying with nitrogen.
The device under test is then glued to the fluidic manifold using the Epox-eez EE4460 from Cotronics. That epoxy was used for its thermal resistance and very low viscosity allowing infiltration in the thin gaps between the device under test and the manifold. The width of the walls between the channels was made to be 0.6 mm. Through characterization, this insures that a sufficient amount of epoxy is present on the walls to fill gaps and defects without over flowing in the device's channels.

The manifold was then glued on the Interposer PCB using a regular, of the shelf, 5 minute epoxy (Figure 2).

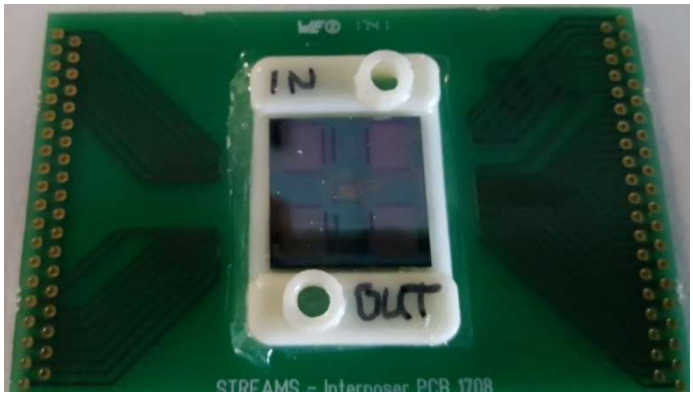


Figure 2 – Assembled device with fluidic stacking having uTES at the top (packaged to CEA) installed on an auxiliary PCB.

The adaptive fins and microvalves integrated on a common lead assembled by adhesive bonding on the backside of the thermoelectric structures consisting of metallic interconnects by CEA-LETI. The final prototype demonstrator was integrated only with µTES, and not with µTEG, given risk level and additional thermal resistance that is expected from µTEG. More details about the TE sensor test structures characterization is presented in WP3. Figure 3 shows the schematic representation of the wire bonding profiles for the TTC4 made at CEA-LETI. The demonstrator also consists of thermal test chips (TTC) provided by STMicroelectronics mounted (by gluing) on to the µTES to form a multi-chip assembly. The glued chips were wire bonded (at CEA-LETI) between the interposer electronic pads and the auxiliary PCB. The power supplied to the heating chips will be provided on the auxiliary PCB of the interposer. TTC 4 has been chosen to use at hot source, depending on the fins and microvalves. Six µTES (4-6-8-10-11-12) have been connected to measure the thermal flow in both directions. The power into the TTC has been controlled by current or voltage, and measurements have been performed in both steady state and transient modes, as reported in WP3 section.

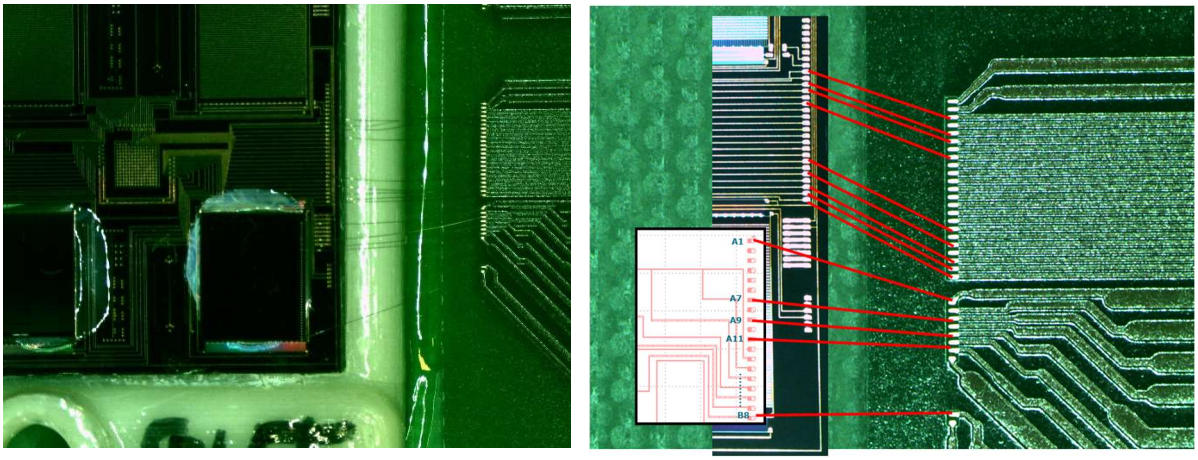


Figure 3 – Schematic representation of the wire bonding profiles for the thermal test chip 4 (CEA).

2 – Methodology

The final demonstrator has been characterized at UdL and its thermal performance was evaluated quantitatively. In a first phase, two functionalities have been validated: cooling system demonstrator (WP2) embedded with µTESs (WP3). The benefits of STREAMS technology on the final thermal map

under different use-cases will be demonstrated, looping the industrial IC design tools with the complete thermal model developed with in the project.
The experimental works associated to this WP5 have been developed at UdL, in collaboration with

- HSG in a first stage, for the black box integration
- LN2. Along the WP5 activities, a straight collaboration and a weekly communications have been implemented between LN2 and UdL.
- CEA assembled the interposer and the auxiliary PCB
- STREAMS consortium. A Joint measurement day (19/06/2019), before M42 General Assembly in Lleida, allowed to implement the last measurements (Figure 4).

Figure 4 – STREAMS consortium for PoC tasks.

2.1 – Test bench

The schematic design of the experimental setup used for this study is shown in Figure 5.

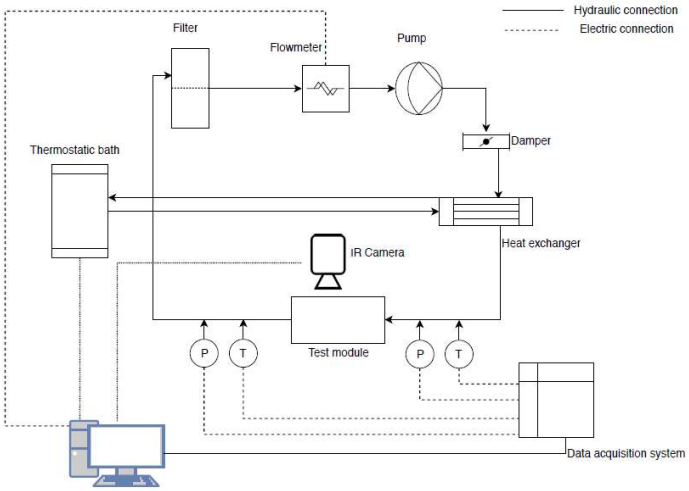


Figure 5 – Test module setup.

The experimental setup is based on two separated hydraulic circuits. In the first one, the water is stored in a thermostatic bath (PolyScience PD07R20-20-A12E) which is thermally connected to the heat exchanger responsible for heating or cooling the water of the second circuit. This second circuit is composed of a 1 µm filter (Shelco MPX) connected to a flowmeter (Bronkhorst mini cori-flow M15) and then to a micro-diaphragm liquid pump (KNF NF5). A diaphragm pulsation damper (KNF FPD06/1.06-

Z), placed after the pump, is responsible for flow stabilization before it enters the heat exchanger. Then, the test module is hydraulically connected to the heat exchanger and finally the water returns to the filter. Type T thermocouples are used to measure inlet and outlet water temperatures and two pressure sensors measure the pressure drop across the device.
Finally, an infrared camera (Flir A655sc) is used for measuring the surface temperatures of the test module. A data acquisition system (Agilent 34970A) collects the information from the test bench and send them to the computer, where LabVIEW software is used to process it (Figure 6).

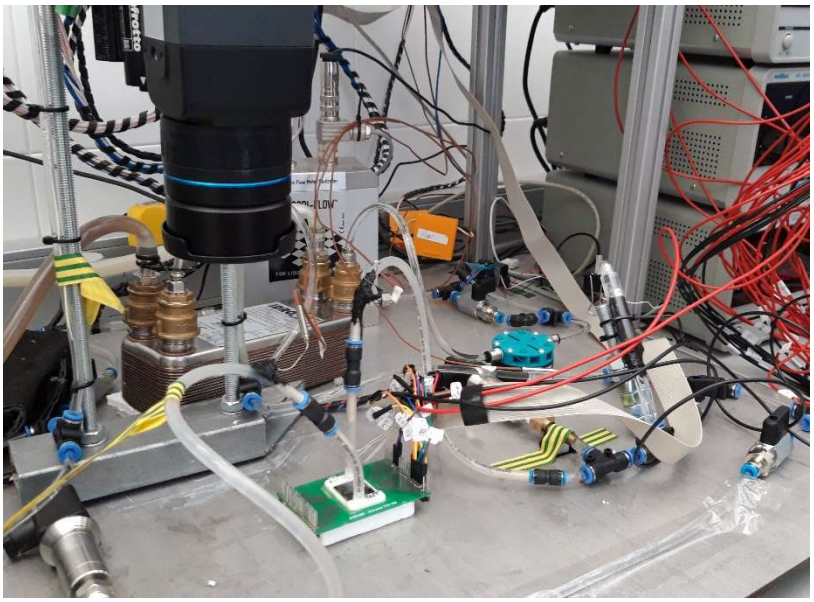


Figure 6 – Test module in UdL Lab.

2.2 – Characterization set up

As illustrated in Figure 7, TTC4 will be used at hot source (depending on fins and valves characteristics measured by LN2, TTC4 has been chosen).
Six µTES (4-6-8-10-11-12) will be connected to measure the thermal flow in the both directions. The scenario consists in activating TTC4 at t = 0s, then activating the cooling system.
The objective is to see the decrease of the thermal flow measured by µTES when the cooling system is activated.

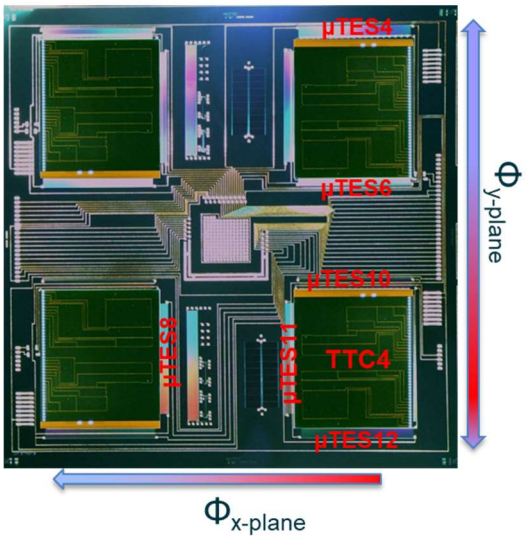


Figure 7 – Picture showing the scenario used for the final demonstrator test.

3 – Results

3.1 – µTES performance

Only the signal coming from µTES8 was measured. Indeed, unfortunately, some wirebondings came off during the travel of sample between CEA and UdL making impossible to acquire data from other µTES. Thus, Figure 8 shows the final assembled active cooling demonstrator tested, having adaptive fins and microvalves and integrating the two functionalities (adaptive microfluidics and thermoelectrics) to evaluate their thermal performance. The overall objective is to see the decrease of the thermal flow measured by µTES8 when the cooling system is activated.

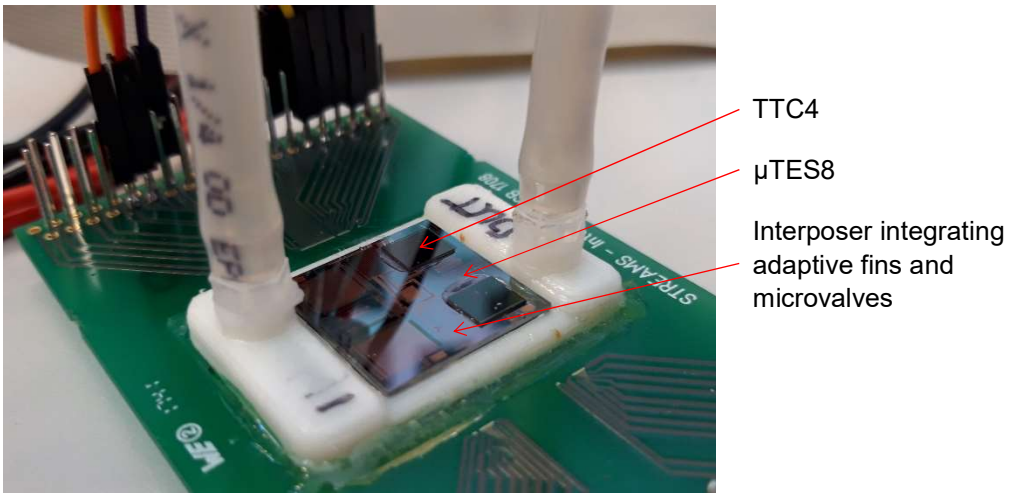


Figure 8 – Picture showing the final assembled active cooling demonstrator integrating two functionalities.

The heater TTC4 was supplied at 150 mA. The pump control voltage values were fixed at 0.5V, 1V and 1.5V for 30 seconds each, then 10s of pumping power off. The flow rate profile is presented in Figure 9.

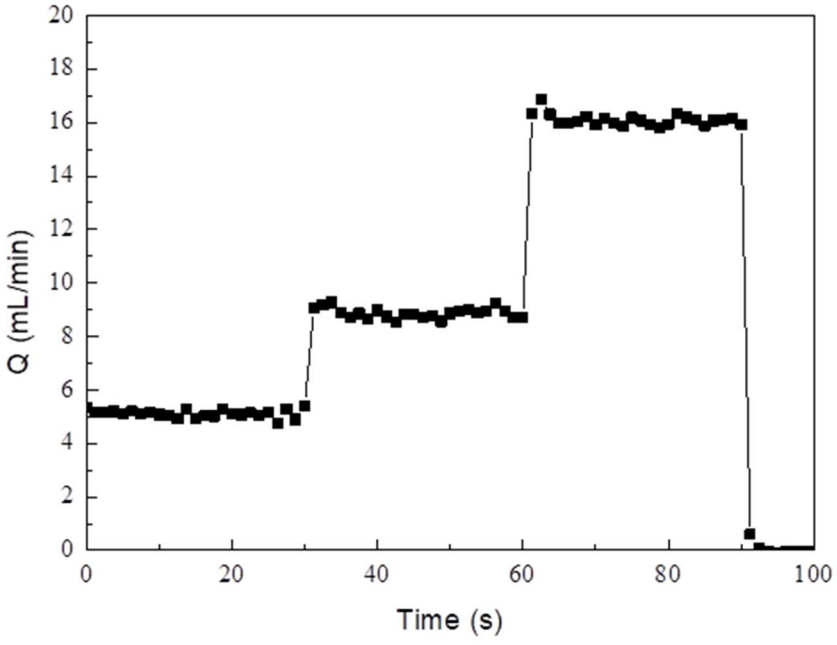


Figure 9 – Flow rate scenario used.

The voltage generated by µTES8 is given in Figure 10 below, as well as its corresponding temperature difference (given by the relation $V_{\mu TES} = N \times S_{np} \times \Delta T$, where N and S_{np} correspond to the µTES junction number and the Seebeck coefficient of one junction, respectively). As already presented in deliverables D3.4 and D3.6, the factor $N \times S_{np}$ equals 110 mV/K for SiGe-based µTES.
It can be seen that the evolution of the voltage and temperature difference corresponds perfectly to the one of pumping flow. Indeed, when the pumping power increases, the TTC4 is cooled and the temperature difference across the µTES8 decreases.
Figure 11 represents the time dependence of T_{TTC4} temperature, pumping power and µTES8 temperature difference. Here again, it can be seen the good correspondence between these three parameters: when the pumping power is low (Q ≈ 5 mL/min), the temperature of TTC4 increases and the µTES8 temperature difference too. When the pumping power increases (Q ≈ 9 mL/min), the temperature of TTC4 decreases, showing the influence of the cooling system, and this decreases is well sensed by the µTES8 ($\Delta T_{\mu TES8}$ decreases too). The same behaviours are obtained when the pumping power increases up to 16 mL/min.

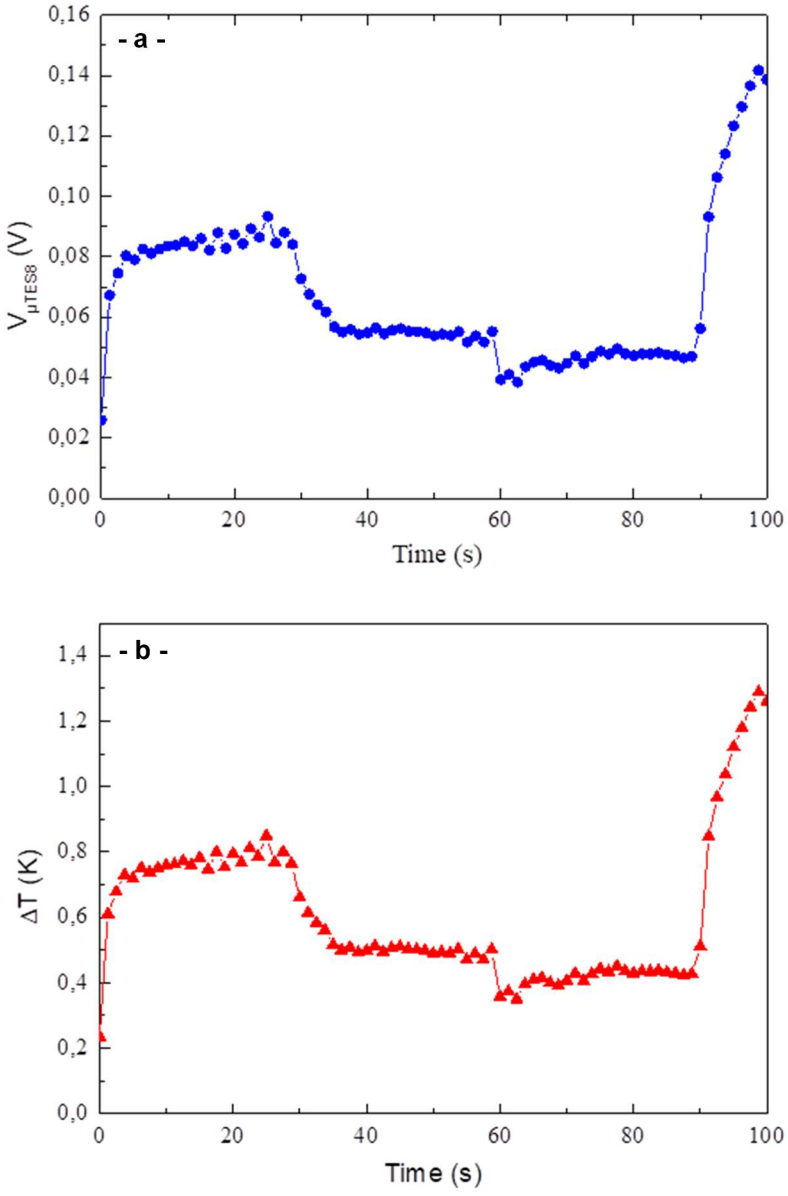


Figure 10 – Time dependence of µTES voltage $V_{\mu TES8}$ (a) and corresponding temperature difference ΔT (b).

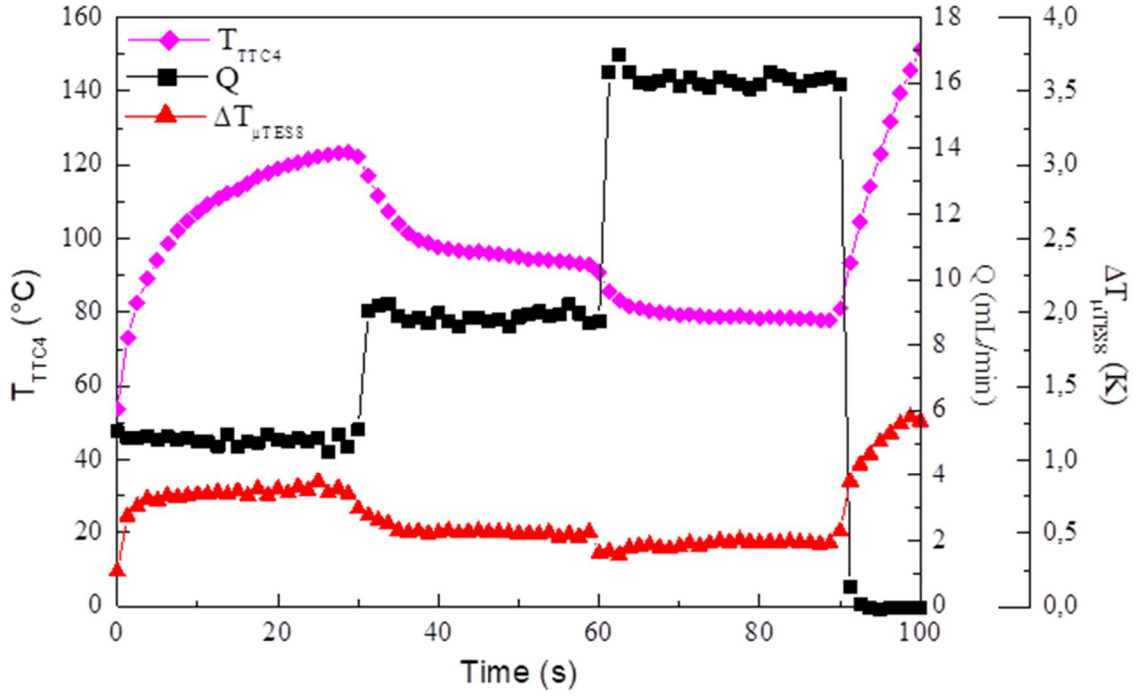


Figure 11 – Time dependence of TTC4 temperature T_{TTC4}, pumping power Q and µTES temperature difference $\Delta T_{\mu TES8}$.

3.2 – Correspondence between µTES signal and thermal analysis

In order to validate the data measured by µTES8, they have been compared to temperatures obtained by thermal infrared images. Indeed, measurements have been filmed with an IR camera, enabling to know the temperature at the µTES extremities, as shown Figure 12 below. In this Figure, Line 1 (in red) and Line 2 (in green) represents the both extremities of µTES8. The temperature difference ΔT_{IRcam} is then obtained by the formula $T_{Line2} - T_{Line1}$.

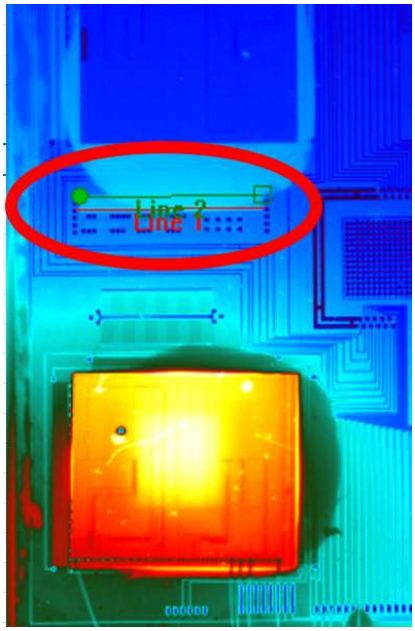


Figure 12 – Thermal image of the interposer showing how is obtained the temperature difference across µTES8 by IR images.

For example, Figure 13 presents IR pictures of the interposer at different time, corresponding to different pumping power (corresponding to the scenario presented in Figure 9).

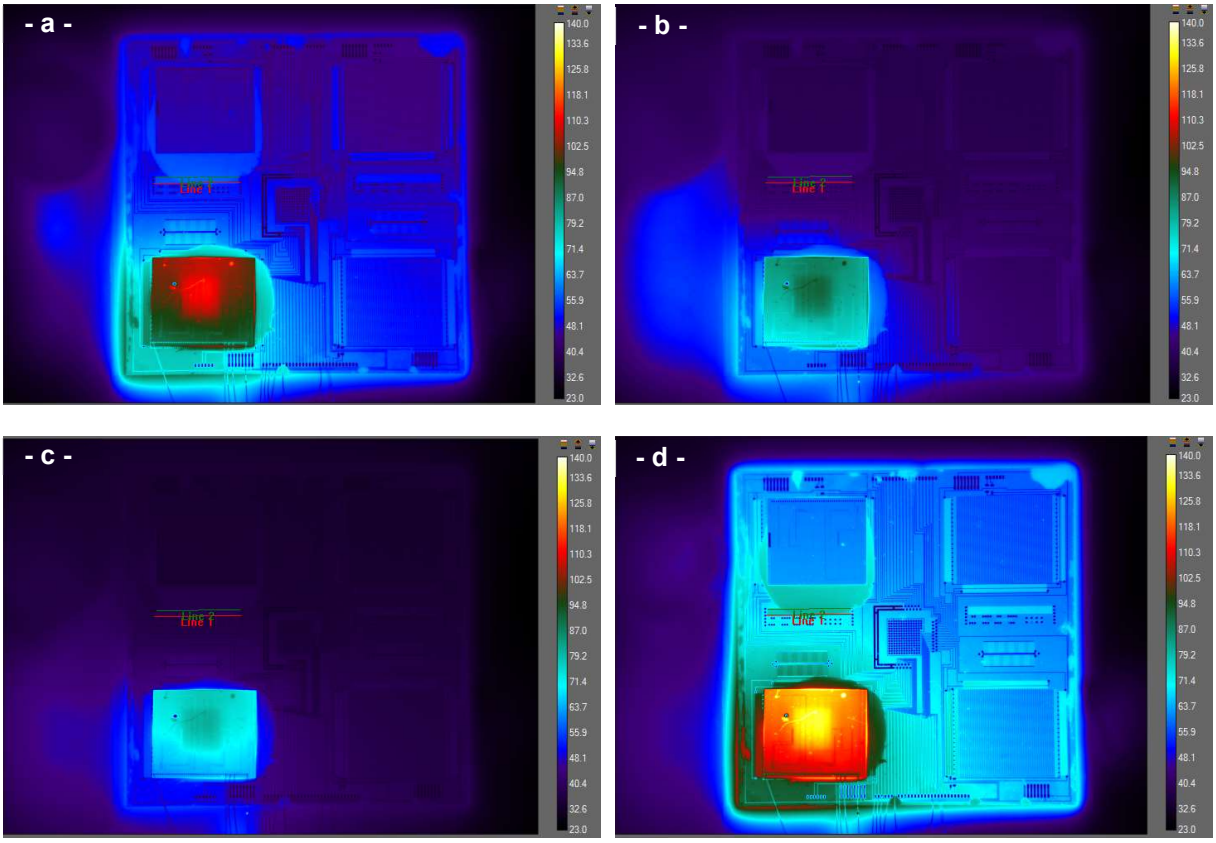


Figure 13 – Thermal image of the interposer at a) t = 30s (P_{pump} = 0.5 V); b) t = 60s (P_{pump} = 1 V); c) t = 90s (P_{pump} = 1,5 V); d) t = 100s (P_{pump} = 0 V);

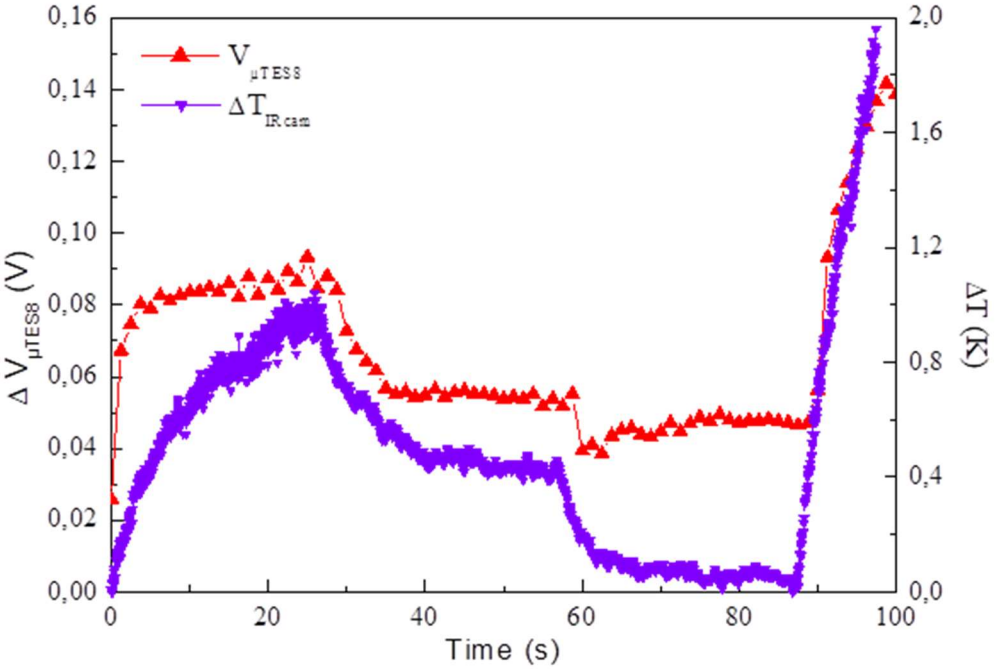


Figure 14 – Comparison of the temperature difference obtained by thermal image ΔT_{IRcam} with the temperature difference measured by µTES8 $\Delta T_{\mu TES8}$.

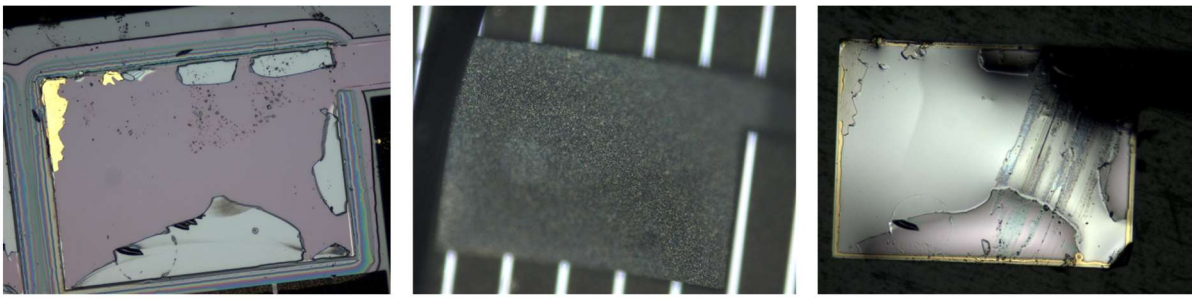
Figure 14 presents the comparison of the temperature difference obtained by thermal image ΔT_{IRcam} with the voltage generated by µTES8 $V_{\mu TES8}$.
It can be well seen that the evolution of both curves fits well, demonstrating that µTES responds perfectly to the different cooling system scenario.

4 – Reliability

Reliability of microelectronic assemblies is largely affected by stresses induced by relative thermal expansion of the chips, substrates and interconnect materials. Here we list the issues of reliability of devices and the microfluidic components (such as interconnects, integrated microvalves, packaging etc.,), along with other limitations such as difficulties encountered in the assembly of the complete active cooling demonstrator. The two main objectives are: identifying the most important problems when it comes to reliability of microfluidic devices and finding out the solutions to how the industrial end-users could deal with these problems.

4.1 – Nickel adhesion on SiO2

It is well known in microfabrication that to get a good adhesion on SiO_2, an adhesion promotion layer should be used. Due to the low chemical reactivity of noble metals such as Au, Ag, Pt, they adhere poorly to the substrate, leading to phenomena like delamination, peeling, and time-dependent device performance deterioration. For such layers, we have chosen chromium (as an adhesion layer) as it is compatible with our process in the fabrication of microheater chips (Refer to WP2). That layer was followed by an Au layer and the main nickel layer to form the metallic serpentine. However, our process exposes these metal layers to high temperatures during the bonding process. It was found that the metal adhesion became very weak following that step. This led to a major reliability issue leading to losses of heater and wire bonding issues. Figure 15 shows the delamination of nickel pads from SiO_2 layer. We hypothesize that, this might be due to a possible diffusion of the chromium and gold layers leading to the loss of the adhesion layer. To remedy that situation, a layer of protective oxide was added over the metallization to reduce this delamination.



Delaminated pad area (Top view of the heater) | Delaminated pad – Nickel surface | Delaminated pad – Backside of the Nickel surface

Figure 1**5** – Pictures showing the delamination of nickel pads from SiO_2 layer.

4.2 – Reliability testing of sealing between the fluidic chip and the plastic manifold

Due to the way the chip is placed on top of the manifolds walls, we had to make sure that the seal was reliable as any fluid passing directly between channels would not contribute to cooling and affect the validity of our results. To test the reliability of the assembly method, several assembly test where made using a clear glass sample and fluids with food coloring agents. Once the manifold wall thickness was tuned to retain the proper amount of glue, the reliability was further tested on silicon samples. The reliability was measured visually and by pressurizing the devices.
Furthermore, after the assembly of each device, a general leak test was performed by slowly pressurizing the device up to 1 bar with water. Any leaks found were sealed using an UV cure resin. The devices were repeatedly tested this way until no leaks were found. It was found that most leaks

were situated in areas subject to stress during assembly, such as the threads for the barbed connector. Through careful manipulation and design improvement, the reliability passed from every device having systematically more than one leaking area to only one leaking area out of three devices. Going forward towards applications, sealing of the chip to the fluidic distributor will require further improvements.

4.3 – Reliability test of wire bonding

The wire bonding of aluminum wires to the nickel pads was found not to be very strong on some samples. We initially suspected that this was caused by the presence of a nickel oxide layer readily formed on the nickel at room temperature. Rather, further reliability testing pointed towards a weak adhesion on rougher nickel surfaces. Such roughness was caused during the electrodeposition of thicker Ni layer (>1.5 µm) or when there was an excessive chemical attack of the nickel layer. It is hypothesized that the nickel being less ductile than the usual aluminum or gold pads, the roughness cannot be deformed by the ultrasound welding probe and therefore lead to an incomplete adhesion of the wire bond to the tip of the roughness.
As shown in Figure 16, it was found that a simple mechanical polishing of the nickel pad using 0.3 µm alumina particles in water was enough to get a proper bonding on the pads. However, such mechanical polishing is laborious, tedious and subject to a high quantity of defects due to the already weak bonding of the nickel layer to the substrate. Instead, the preferred method was to use a thinner layer of nickel. This led to a higher electrical resistance of the heaters.
Finally, the success of the wire bonding of each device was measured by testing the resistivity of each heater present on each device. Through design improvement, the reliability passed from less than 10% reliable connection to more than 80% of the heater functioning. The rest of the dysfunctional heaters were usually caused by the delamination of the pads or heater themselves.

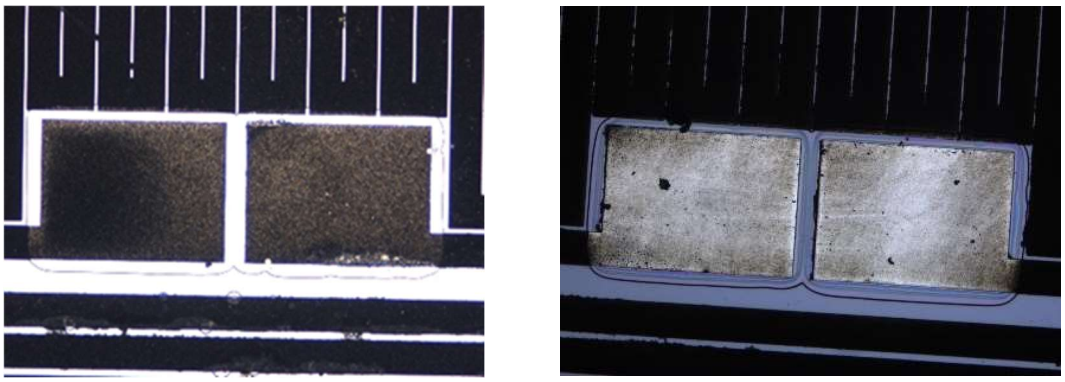


Figure 16 – Optical microscopic images showing the unpolished (left side) and polished (right side) nickel pads.

4.4 – Reliability of the wire bonding encapsulation

Due to the long length of the wire bond used and the fact that the samples needed to be shipped around labs, it was imperative to protect the wire bonds by encapsulation. The initial solution was using an acrylic based UV curable resin and covering all of the wire with it. Figure 17 shows the wirebondings between auxiliary PCB and thermal heater chips completely covered by using UV resin. However, it was found that electrical connections became intermittent during heating and cooling of the devices. Further analysis and reliability test lead to the hypothesis that the intermittent connection was likely caused by a major thermal expansion mismatch between the resin used and the silicon substrate of the sample.

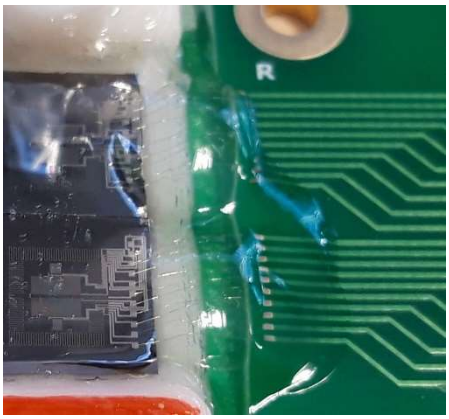


Figure 17 – Picture showing the wire bonding completely covered by UV curable resin.

Instead of using this rigid resin, it was chosen to use a flexible polydimethylsiloxane resin and to cover only half of the bond with it. The flexibility of the resin allows it to distribute the stresses around by deforming. The fact that the silicon chip is not covered also helps lower the deformation since it is the area subjected to the highest temperatures under test. Until now, there was not any reports of unreliable connections using this technique.

4.5 – Reliability assessment of the valves

The reliability assessment of the valves consisted of cycling the valve aperture. The valves have been operated until achieving 1000 cycles without observing (qualitatively) variations of the valve behavior.

4.6 – Issues encountered for the µTEG on daughter board characterization

Wire bonding issues:

- Bond wires embedded in epoxy lifted when heating power from TTC turned ON.

Mechanical issues:

- Daughter board twisted when installed/removed from the support
- Interposer taken off PCB on µTES SiGe sample
- Solution: carefully align the pins before soldering

Mechanical impact of this twist probably also impacts epoxied wires, as illustrated in Figure 18.

These challenges can be circumvented with improved packaging processes.

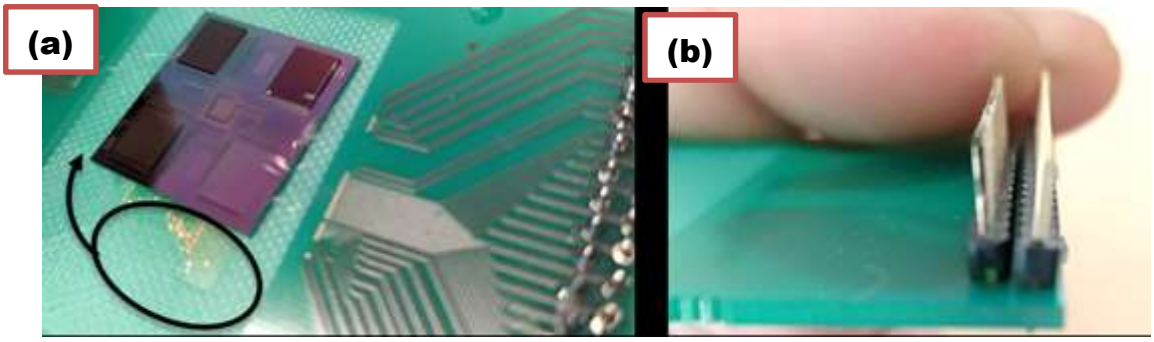


Figure 18 – (a) picture of interposer taken off PCB (uTES) and (b) Misaligned pins.

5 – Conclusions and future works

It was shown in this report the characterization of the final demonstrator developed in the project STREAMS. Even if only two functionalities in three were tested, the results obtained both for the cooling system and the thermal sensor are very good and coherent.

We have demonstrated that we will be able, after some additional works and calibrations, to correlate the temperature map to the µTES signals. It demonstrates that the integration of these two STREAMS functionalities is meaningful, as, in other STREAMS tasks, we have demonstrated that the STREAMS cooling solution is able to reduce drastically the pumping power by tailoring the total flow rate to the chip temperature distribution.

Originally, we planned to measure six µTES in this demonstrator, but due to wirebondings issues, only one µTES was available. UdL and CEA are greatly motivated to perform new tests with all µTES connected. In this way, UdL will send back the sample to CEA. CEA will repair the wirebondings and the sample will be send again to UdL. The measurement of the demonstrator with all µTES functional, combined with the IR camera, will enable to have a full functional system and to perform temporal analysis. Indeed, it will be interesting to compare the six µTES response times, in correlation with their distance from the TTC. The team plans also to publish these significant results in a high-level journal.